PEOPLE'S DEMOCRATIC REPUBLIC OF ALGERIA
MINISTRY OF HIGHER EDUCATION AND SCIENTIFIC RESEARCH

YAHIA FARES UNIVERSITY OF MEDEA

Faculty of Technology

Department of Electrical Engineering

Master's dissertation

Branch : Telecommunications.

Option : Telecommunication Systems.

DESIGN AND SIMULATION OF A HOMODYNE FM RECEIVER BASED ON A FRACTIONAL ORDER PLL

Presented by:

BADREDDINE GACEM

YASSINE HAZI

Proposed and Directed by:

Mr. Noureddine Batel

Mr. Billel Essaid

Promotion 2024

Acknowledgments

We would like to express our sincere gratitude to:

- Our supervisors, Mr. Noureddine Batel and Mr. Billel Essaid, for their invaluable guidance, support, and encouragement throughout the course of this research.
- The faculty and staff of the Department of Telecommunications at Yahia Fares University of Medea for providing resources and facilities essential to the completion of this dissertation.
- Our colleagues and friends for their understanding, encouragement, and moral support during challenging times.
- Our families for their unwavering love, encouragement, and belief in our abilities.

Their contributions have been instrumental in the completion of this dissertation, and we are deeply thankful for their support.

الملخص

العالي جدًا (VHF). يجمع التصميم المفصل وتحديد حجم المكونات الأساسية للدائرة بين التحليل النظري والتنفيذ العملي عبر المحاكاة. تشمل الجوانب الرئيسية التي تم تغطيتها مثل كاشفات الطور، والمرشحات المنخفضة التمرير، والمذبذبات التي يتم التحكم فيها بواسطة الجهد (VCOs)، لضمان فهم شامل لأدوارهم ومقاييس أدائهم. يتم إجراء قياسات في المجال الزمني لتقييم سلوك PLL في تكوينات الحلقة المفتوحة والمغلقة. تكشف المحاكاة عن استجابات عابرة تليها نظام ثابت، مما يبرز قدرة PLL على إزالة التضمين بشكل فعال للإشارات FM المستقبلة. تظهر النتائج أنه في الحلقة المغلقة، تقل الفولتية الطفيلية وتثبت استقرار PLL. على الرغم من أن تصميمات PLL ذات الترتيب الكسري لم يتم تضمينها بسبب قيود الوقت، إلا أن الدراسة توفر رؤى قيمة حول دوائر PLL التقليدية ذات الترتيب الصحيح. تُعد هذه الدراسة أساسًا قويًا للتقدم المستقبلي في أنظمة الاتصالات FM، مما يبرز أهمية التصميم المدعوم والمحاكاة الدقيقة في تحسين أداء PLL.

الكلمات المفتاحية: الحلقة المغلقة، التردد العالي جدًا، إزالة التضمين المتجانس، Pspice.

Résumé

Ce mémoire explore la conception et l'analyse des performances des circuits à boucle à verrouillage de phase (PLL) dans les systèmes de communication FM, donc en VHF. La conception détaillée et le dimensionnement des composants de circuits essentiels, combinent analyse théorique et mise en œuvre pratique par simulation. Les aspects clés couverts tels que les détecteurs de phase, les filtres passe-bas et les oscillateurs contrôlés en tension (VCO), assurent une compréhension globale de leurs rôles et de leurs métriques de performance. Des mesures dans le domaine temporel, évaluant le comportement de la PLL dans des configurations en boucle ouverte et en boucle fermée, sont menées. Les simulations révèlent des réponses transitoires suivies d'un régime permanent, mettant en évidence la capacité de la PLL à démoduler efficacement les signaux FM reçus. Les résultats montrent comment qu'en boucle fermée, les tensions parasites se réduisent et que la stabilité de la PLL est établie. Bien que les conceptions de PLL d'ordre fractionnaire n'ont pas été incluses en raison des contraintes de temps, l'étude offre des informations précieuses sur les circuits PLL traditionnels d'ordre entier. Cette étude fait office de base solide pour les futures avancées dans les systèmes de communication FM, soulignant l'importance de la conception assistée et de la simulation précise dans l'amélioration des performances de la PLL.

Mots clés: PLL, VHF, Démodulation homodyne, PSpice.

Abstract

This thesis explores the design and performance analysis of Phase-Locked Loop (PLL) circuits in FM communication systems, specifically in VHF. The detailed design and sizing of essential circuit components combine theoretical analysis and practical implementation through simulation. Key aspects covered, such as phase detectors, low-pass filters, and voltage-controlled oscillators (VCOs), ensure a comprehensive understanding of their roles and performance metrics. Time-domain measurements, evaluating the PLL's behavior in open-loop and closed-loop configurations, are conducted. The simulations reveal transient responses followed by a steady-state regime, highlighting the PLL's ability to effectively demodulate received FM signals. The results show that in a closed-loop, parasitic voltages are reduced, and PLL stability is established. Although fractional-order PLL designs were not included due to time constraints, the study provides valuable insights into traditional integer-order PLL circuits. This study serves as a solid foundation for future advancements in FM communication systems, emphasizing the importance of assisted design and precise simulation in improving PLL performance.

Keywords: PLL, VHF, Homodyne demodulation, PSpice.

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Glossary

AM	Amplitude modulation
FM	Frequency Modulation
AMPS	Advanced Mobile Phone Service/System
DC	Direct Current
f_{center}	is the center frequency of the VCO when the control voltage V_m is zero
K_V	is the sensitivity of the VCO
V_m	is the control voltage applied to the VCO
dB	decibel
dBC/Hz	power relative to total signal power
dBm	decibel relative to 1 mW (1mW = 0 dBm)
Er	error, noise
Ev	Error Voltage
E(t)	Error Signal
f_m, w_m	modulating frequency
F	fractionality, noise figure
Fr, f_{in}	Input reference frequency
Fo, f_{OUT}	VCO output frequency
Fx	crystal frequency
F(s),	H(s) transfer function
GCD(x,y)	greatest common divisor
Kv VCO	constant, usually in MHz/Volt
Kd	phase detector constant, usually V/rad or mA/rad
L(fm)	single sideband noise density
LD	lock detect
LSB	least significant bit
M, A, N	PLL counters
MSB	most significant bit
m	index of modulation
MC	modulus control
N	division ratio
P	dual modulus basic divider
PFD	phase frequency detector
R	crystal divider
PM	phase modulation
SSB	single side band
VCO	Voltage Controlled Oscillator
T, t, τ	time or time delay
TCXO	Temperature Compensated Crystal Oscillator
ξ	damping factor
ϕ, φ	phase

ϕ_M	phase margin
ωn	natural frequency
ω_0	center or carrier frequency
ωp	frequency where open loop gain equals 1
Vin	Input Signal
Vout	Output Signal
LNA	Low Noise Amplifier
LO	Local Oscillator
BO	Open Loop
BF	Closed Loop
KTB	Power level of white noise

General Introduction

Topic and Context

In the realm of communication systems, frequency modulation (FM) stands as a cornerstone for transmitting information. The Homodyne FM receiver, known for its simplicity and efficiency in demodulating signals directly to baseband, plays a pivotal role in enhancing communication quality and reliability. Integral to its performance is the Phase-Locked Loop (PLL), a feedback control system crucial for frequency synthesis and signal synchronization. This dissertation explores the role of traditional PLLs in optimizing the performance of Homodyne FM receivers, focusing on improvements in phase noise, stability, and bandwidth utilization.

Focus and Scope

This dissertation delves into the design and simulation of a Homodyne FM receiver, emphasizing the theoretical underpinnings and practical implementations of traditional PLL designs. By exploring the mathematical modeling and system design considerations, the study aims to illuminate the comparative advantages of these designs. The scope encompasses mathematical modeling, system design considerations, and simulation-based analysis to evaluate performance metrics such as phase noise, lock time, and frequency stability under varying conditions.

Relevance and Importance

The evolution of communication technologies necessitates continual advancements in the underlying hardware to meet increasing demands for efficiency, reliability, and quality. The exploration of traditional PLLs within Homodyne FM receivers addresses this need, offering potential improvements in performance that could significantly benefit areas such as wireless communication, broadcasting, and data transmission. This research not only contributes to the academic discourse but also provides a foundation for future innovations in communication system design.

Questions and Objectives

The study is guided by the following questions:

- How does the incorporation of a traditional PLL influence the performance of a Homodyne FM receiver?
- What are the specific benefits in terms of phase noise, lock time, and frequency stability?

Objectives include:

- To model and simulate a Homodyne FM receiver integrating a traditional PLL.
- To compare the performance of different PLL designs in the context of a Homodyne FM receiver.
- To identify the optimal design parameters for maximizing the receiver's efficiency and signal fidelity.

Overview of the Structure

The dissertation is structured as follows:

- **Chapter 1** introduces the research topic, outlining its significance and relating the theory to the current state of the art of the subject.
- **Chapter 2** delves into the presentation and sizing of various circuits essential for the practical implementation of different roles and functions in FM communication systems. It covers the theoretical aspects, including detailed equations and simulation profiles, to provide a comprehensive understanding of the underlying mechanisms and their performance metrics.
- **Chapter 3** provides and discusses the simulation results in the presence and absence of surrounding noise, while carrying out a comparison between the systems of processed communication using traditional integer-order PLL designs.

Chapitre 1: State of the Art

1.1 Modulation (FM)

Frequency Modulation (FM) is a method of encoding information onto a carrier wave by varying the frequency of the wave in accordance with the amplitude of the modulating signal. In FM, the frequency of the carrier wave is altered in proportion to the amplitude (strength) of the input signal. This means that as the amplitude of the input signal changes, the frequency of the carrier wave changes accordingly. FM is widely used in telecommunications, particularly in radio broadcasting and two-way radio communication systems. It offers several advantages over other modulation techniques, such as:

- **Improved Signal Quality:** FM offers better signal-to-noise ratio compared to Amplitude Modulation (AM), resulting in clearer reception and reduced interference.
- **Resistance to Amplitude Variations:** Since FM relies on frequency changes rather than amplitude changes, it is less affected by variations in signal strength due to factors like distance and interference.
- **Wide Bandwidth Efficiency:** FM signals occupy a wider bandwidth compared to AM signals, allowing for the transmission of more information in a given frequency range.

FM modulation is also used in various other applications including television broadcasting, satellite communications, radar systems, and mobile phone networks. Its ability to provide high-quality transmission with resistance to noise and interference makes it a versatile and widely used modulation technique in modern communication systems[16] [17] .

1.2 The importance of FM modulation

Frequency Modulation (FM) is a crucial modulation technique widely used in communication systems for its superior audio quality, resistance to noise and interference, and versatility. It offers high-fidelity audio transmission, making it ideal for radio broadcasting, music transmission, and two-way communication systems. FM modulation ensures reliable communication in challenging environments and finds applications in broadcasting, telecommunications, data transmission, radar systems, and military communication. Its ability to deliver clear and reliable signals has made it an indispensable technology in modern communication infrastructure[18] [19].

1.3 Introduction to Phase Locked Loop (PLL)

PLL Operation [13] goes through 3 states:

- Free running.
- Capture.
- Phase Lock.

1.3.1 Free running

If no input is applied, the PLL is in free running state.

$f_{OUT} = f_{center}$ $(input\ is\ 0)$

1.3.2 Capture

- Once the input is applied , VCO frequency starts to change and PLL is said to be in the Capture mode (Capture the input frequency f_{IN})
- It is referred to as “frequency pull in”.

1.3.3 Phase Lock

- The lock range is defined as the range of frequency over which the change of input frequency f_{IN} and output frequency f_{OUT} is zero($f_{IN} - f_{out} = 0$), then it is referred to as Phase Lock..

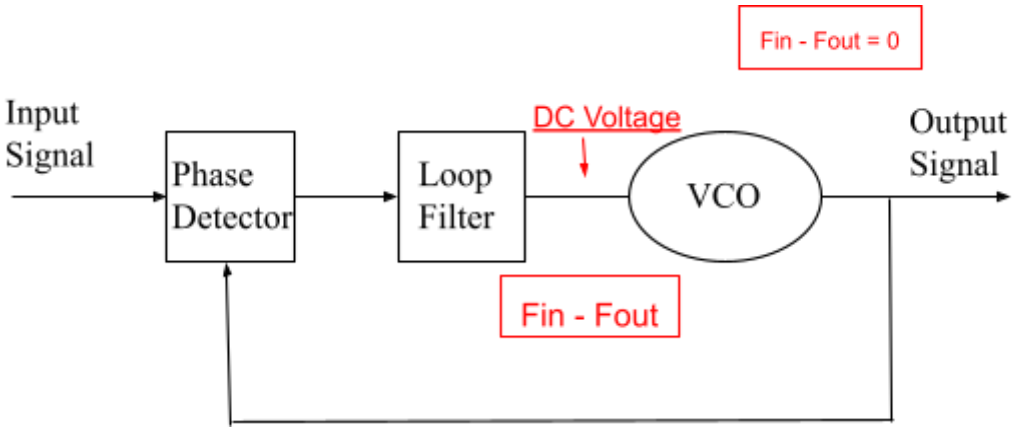


Figure 1.1: Operation of PLL

1.3.4 Applications

- FM coherent demodulation
- AM coherent demodulation

These are basic applications where we could use this PLL.

1.4 Frequency Synthesis

Frequency Synthesis [5] is the engineering discipline dealing with the generation of multiple signal frequencies, all derived from a common reference or time base. The time base used is typically a Temperature Compensated Crystal Oscillator (TCXO). The TCXO provides a reference frequency to the synthesizer circuit so that it may accurately produce a wide range of signals that are stable and relatively low in phase noise.

1.5 Digital PLL Synthesis

Among the many different frequency synthesis techniques, the dominant method used in the wireless communications industry is the digital PLL circuit. While there are some benefits to using other synthesis techniques, they are outside the scope of this document and will not be discussed here.

1.6 Integer-N PLL

Compared to the analog techniques used in the infancy of frequency synthesis, the modern PLL is now a mostly digital circuit. Figure 1.2 shows a typical block diagram of a PLL implemented with a TCXO reference.

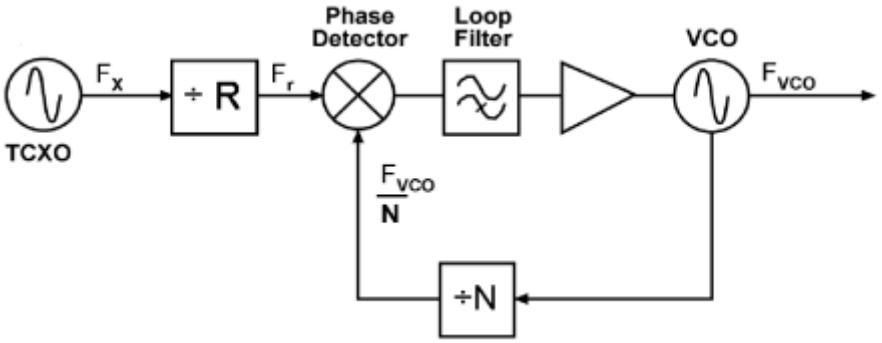


Figure 1.2. Integer-N (classical) PLL Block Diagram

This traditional digital PLL [5] implementation will be termed "integer-N" to avoid confusion due to the addition of fractional-N technology. The PLL circuit performs frequency multiplication, via a negative feedback mechanism, to generate the output frequency, Fvco, in terms of the phase detector comparison frequency, Fr.

$$Fvco = N \bullet Fr \quad \text{.....(1.1)}$$

To accomplish this, a reference frequency must be provided to the phase detector. Typically, the TCXO frequency (Fx), is divided down (by R) "on-board" the PLL IC. The phase detector utilizes this signal as a reference to tune the VCO and, in a "locked state," it must be equal to the desired output frequency, Fvco, divided by N.

$$Fvco / N = Fx / R = Fr \quad \text{.....(1.2)}$$

Thus, the output frequency that the synthesizer generates, Fvco, can be changed by reprogramming the divider N to a new value. By changing the value N, the VCO can be tuned across the frequency band of interest. The only constraint to the frequency output of the system is that the minimum frequency resolution, or minimum channel spacing, is equal to Fr.

$$Channel\ spacing = Fvco / N = Fr \quad \text{.....(1.3)}$$

When the PLL is in unlocked state (such as during initial power up or immediately after reprogramming a new value for N) the phase detector will create an error voltage based on the phase difference of the two input signals. This error voltage will change the output frequency of the VCO so that it satisfies Equation-(1.2). As long as the system is in a locked condition the VCO will have the same frequency accuracy as the TCXO reference. If the crystal accuracy is 1 part-per-million (ppm), the output frequency of the synthesizer will also be accurate to 1 ppm. Specifically, if Fr = 30 kHz and N = 32000, the only way for this circuit to be in a stable state (locked) is when Fvco = 960 MHz. If N were changed to 32001, a frequency and phase error will develop at the input of the phase detector that will, in turn, retune the VCO frequency until a locked

state has been reached. The locked state will be reached when Fvco=960.03MHz and, if the TCXO has an accuracy of 1ppm, the output of the VCO will be accurate to ~ +/- 960 Hz.

1.7 Fractional-N PLL

An unavoidable occurrence in digital PLL synthesis [5] is that frequency multiplication (by N), raises the signal's phase noise by 20Log(N) dB. The main source of this noise is the noise characteristics of the phase detector's active circuitry. Because the phase detectors are typically the dominant source of close-in phase noise, N becomes a limiting factor when determining the lowest possible phase noise performance of the output signal.A multiplication factor of N = 30,000 will add about 90 dB to the phase detector noise floor. 30,000 is a typical N value used by an integer PLL synthesizer for a cellular transceiver with 30kHz channel spacing. It would seem that we could radically reduce the close-in phase noise of our system by reducing the value of N but unfortunately the channel spacing of an integer-N synthesizer is dependent on the value of N (see Equation 1.3) Due to this dependence, the phase detectors typically operate at a frequency equal to the channel spacing of the communication system.

A phase detector is a digital circuit that generates high levels of transient noise at its frequency of operation, Fr. This noise is superimposed on the control voltage to the VCO and modulates the VCO RF output accordingly. This interference can be seen as spurious signals at offsets of +/- Fr (and its harmonics) around Fvco. To prevent this unwanted spurious noise, a filter at the output of the charge pumps (called the loop filter) must be present and appropriately narrow in bandwidth. Unfortunately, as the loop filter bandwidth decreases, the time required for the synthesizer to switch between channels increases.

For a 2nd order loop with natural frequency (loop bandwidth) ωn and damping factor ξ, the switching speed (Tsw) is proportional to the inverse of their product.

$$Tsw \; \alpha \; 1/\omega n\xi \qquad \text{.....(1.4)}$$

If N could be made much smaller, Fr would increase and the loop filter bandwidth required to attenuate the reference spurs could be made large enough so that it does not impact the required switching speed of our system. Once again, however, the upper limit of Fr is bound by our channel spacing requirements. This illustrates how our desires to optimize both switching speed and spur suppression directly conflict with each other.

A newly emerging PLL technology has made it possible to alter the relationship between N, Fr, and the channel spacing of the synthesizer. It is now possible to achieve frequency resolution that is a fractional portion of the phase detector frequency. This is accomplished by adding internal circuitry that enables the value of N to change dynamically during the locked state. If the value of the divider is "switched" between N and N+1 in the correct proportion, an average division ratio can be realized that is N plus some arbitrary fraction, K/F. This allows the phase detectors to run at a frequency that is higher than the synthesizer channel spacing.

$$Fvco \; = \; Fr \; (N \; + \; K \; / \; F) \; N, \; K, \; F \; are \; integers \qquad \text{.....(1.5)}$$

Where: F = The fractional modulus of the circuit (i.e. 8 would indicate a $1/8^{th}$ fractional resolution.)
K = The fractional channel of operation.

1.8 Evolution of Phase-Locked Loop (PLL) Technology

Among today's System-on-Chip (SOC) integrated circuits, Phase-Locked Loops (PLLs) stand as ubiquitous analog/mixed-signal components, serving as indispensable companions to the digital-logic circuits and processors embedded within these chips. The integration of multiple PLLs has become commonplace in modern SOC designs, reflecting the ongoing advancements in process technology that benefit analog/mixed-signal circuits. Through innovative design approaches, engineers have significantly enhanced the performance of PLLs, surpassing conventional expectations of mere scaling. These advancements in process technology and circuit techniques have resulted in smaller PLL footprints with reduced power consumption per megahertz of output frequency, along with superior overall performance compared to PLLs of previous decades. Such progress has enabled a wide array of applications for PLLs, encompassing functionalities such as Serializer/Deserializer (SERDES) circuits—specialized circuits facilitating high-speed data transmission over communication links with minimal physical channels—and seamless integration with Radio Frequency (RF) systems [15].

1.8.1 A bit of history

Phase-locked loops (PLLs) have been influential since the 1920s, significantly advancing with the development of monolithic PLLs. A key milestone in the 1970s was the introduction of the 4046.CMOS Micropower PLL by the Radio Corporation of America (RCA), one of the first integrated circuit (IC) implementations of PLL technology. This device became essential for applications such as **frequency synthesis**, **FM demodulation and modulation**, **voltage-to-frequency conversion**, and **data synchronization**. Frequency synthesis involves generating a range of frequencies from a fixed base frequency. FM demodulation and modulation adjust the carrier signal frequency according to the transmitted information, like voice or data. Voltage-to-frequency conversion translates input voltage into a corresponding frequency output, useful in analog-to-digital conversion processes. Data synchronization ensures data transfer timings between multiple devices or components in electronic systems are coordinated to maintain data integrity and accuracy.

The 4046 PLL included two types of phase detectors: a linear mixer, producing an output signal proportional to the cosine of the phase difference between two input signals, and an edge-triggered phase/frequency detector, which responds to transitions (edges) from high to low or low to high, making it useful for detecting both phase and frequency differences. These phase detectors worked together with a voltage-controlled oscillator (VCO) and an output buffer. This setup allowed designers to use the tuning voltage for frequency control and demodulation applications, thereby enhancing the device's versatility.

The flexibility of the 4046 PLL was a significant feature of its design. With an external divider, designers could reconfigure the circuit as a versatile frequency synthesizer capable of generating frequencies from tens of kilohertz to just over 1 MHz. Despite this wide frequency range, power

consumption remained minimal, ranging from microwatts to 1 milliwatt. Additionally, the inclusion of an external loop filter, although initially perceived as an extra step, provided designers the flexibility to finely adjust the loop dynamics to meet specific application requirements precisely. An external divider, a crucial component within PLLs, reduces the frequency of a signal by a predetermined factor, making high frequencies more manageable for processing.

1.8.2 Fast-forward to today

The frequency-multiplying PLL emerges as the predominant type for System-on-Chip (SOC) applications, facilitating the generation of high-frequency clocks from low-frequency references like crystals, a type of electronic component used as frequency references in PLLs. They provide a stable and precise frequency signal, typically at a low frequency, which can then be multiplied to generate higher-frequency clocks as needed in SOC applications. These PLLs find extensive use in logic clocking and RF local-oscillator synthesis, with modern SOCs often integrating five to ten of them. Contrasting with older designs like the 4046 chip, an external feedback divider,and the external loop-filter components(Figure 1.3). Modern SOC PLLs exhibit remarkable advancements, boasting significantly reduced footprint—approximately 2000 times smaller—alongside enhanced features. Despite their compact size, these fully integrated PLLs deliver output frequencies up to 2GHz, demonstrating a drastic improvement in power efficiency, nearly 2000 times better in watts per megahertz.

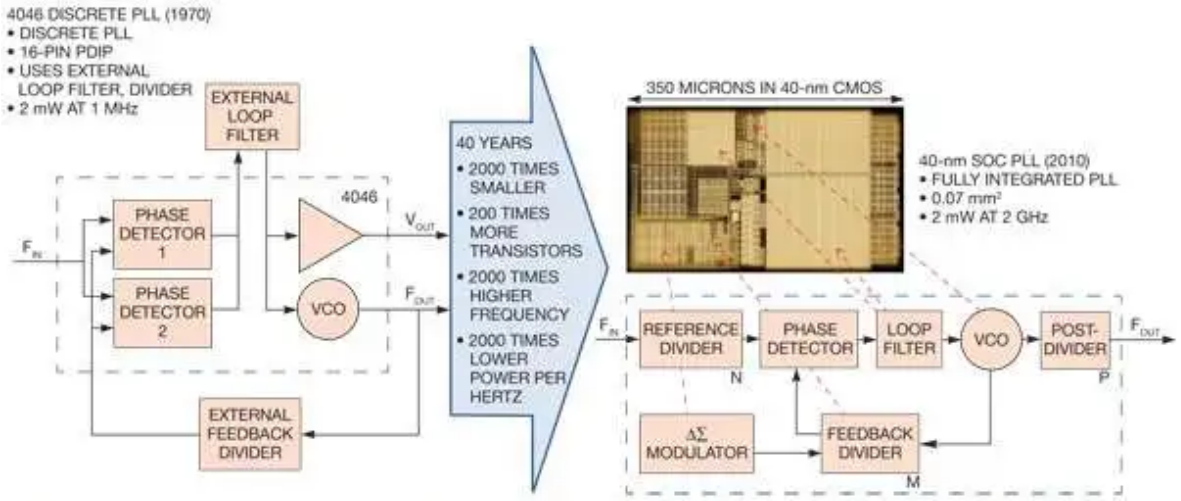


Figure 1.3 Comparing a 1970s PLL (left) to a recent one (right) illustrates the progress that has occurred over the decades.

Advancements in frequency, power efficiency per megahertz, and compactness primarily stem from progress in process technology, aligning with Moore's Law expectations. A comparison between the SOC PLL and the 4046 chip underscores this evolution. While the SOC PLL integrates over 25,000 transistors, the 4046 chip occupied about 5.6 mm² for its 150 components. This exponential increase in transistor count empowers analog/mixed-signal-circuit designers to push the boundaries of performance and creativity [6].

1.8.3 Advances in resolution

Most frequency-synthesis PLLs incorporate a predivider (÷N) and post dividers(÷P), plus a feedback divider (÷M),generating a frequency of:

$$FIN \times M/(N \times P). The\ resolution\ in\ output\ frequency\ is\ FIN\ /(N \times P)$$

Making these dividers larger yields finer resolution. However, this improvement comes at a cost in other important performance parameters.

As N increases, the PLL comparison frequency decreases, and PLL bandwidth must decrease proportionally. A decrease in bandwidth increases the lock time and PLL area—because the loop filter must grow—and the long-term jitter gets worse. Increasing P requires the VCO to run P times faster. A P value of two to four is common for many applications.For large P values, however, the required VCO frequency could exceed the process limitations.

Additionally, the power in the VCO and dividers scales with theVCO frequency. So, using the post divider to achieve fine frequency resolution has serious drawbacks, as well. One way to avoid these trade-offs is to use a non-integer divide value for one of the dividers;fractional-N PLLs employ this approach.

You can achieve a fractional divider value of, for example, 10.25 by the following set of divider values: 10, 10, 10,11, 10, 10, 10, 11, and so on. You can implement such a variable-ratio divider with a simple accumulator (**Figure 1.4** and [7]). Next, you must decide which of the three dividers should be fractional. The first choice—the post divider—has the problem of transferring the noise or jitter of the divider modulation directly to the output—usually,an unacceptable situation. Assuming That the PLL holds the VCO frequency steady, the output period would vary by a whole VCO period. To minimize jitter,the VCO would need a small period, corresponding to a high frequency.

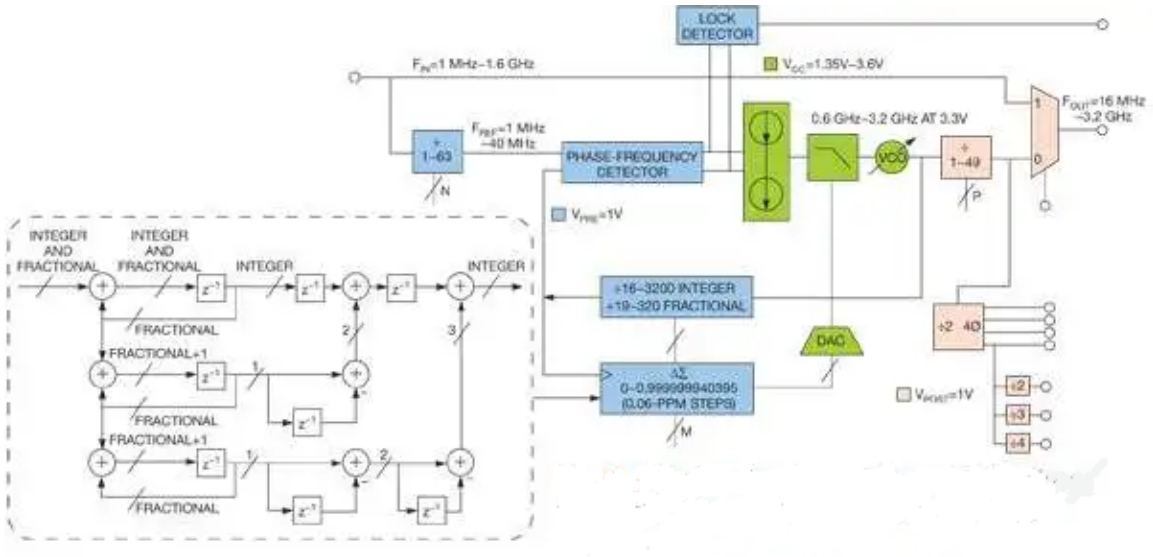


Figure 1.4 The fractional-N divider and delta-sigma modulator represent relatively recent design advances.

The pre divider and post divider are better choices for modulation because,in these configurations, the PLL acts as a low-pass filter on the noise or jitter associated with modulating the feedback divider. The following equation relates the VCO frequency and the reference frequency:

$$FVCO = FREF \times M/N$$

For most practical PLLs, the value of M is larger than that of N, meaning that theVCO period is smaller than the reference period. So, dithering the feedback divider has a smaller effect than dithering the reference divider by the ratio of M/N, making this choice the most common one. Circuits of this type, using multiple ICs, began to appear in the late 1970s and early 1980s.

In the example of the sequence for generating a divider value of 10.25, the divide pattern repeats every four cycles.This approach generates a noise tone at FREF /4. If you use the same method to generate an effective value of 10.01,then a tone would appear at FREF /100.The spectral tone is problematic for many systems that would like to take advantage of the fine frequency resolution that fractional-N PLLs provide.If this noise tone falls to a frequency below the PLL's bandwidth, considerable long-term jitter, unacceptable in many applications, can result.

A breakthrough in the evolution of the fractional-N PLL was the application in 1993 of delta-sigma modulation to the dithering of the feedback divider (**Figure 1.4** and [8]).The delta-sigma-modulation noise-shaping technique can push dithering noise to high frequencies, at which the PILL can easily filter it. Using this technique, designers have created PLL with nearly undetectable fractional spurtones. Integrated fractional-N PLLs still fall short of the performance of similar integer-N PLLs, however, because of the low bandwidth necessary to filter the dithering noise. With lower bandwidth,the PLL is less able to suppress the phase noise of the VCO.

The dithering noise from the delta-sigma modulator is a pseudorandom pattern. A recent refinement integrated PLLs cancels this noise by applying a correction directly to the loop filter. Industry literature reports improvements of 10 to 20 dB, allowing designers to increase the bandwidth of fractional-N PLLs, with benefits in circuit area, phase noise, and jitter. In this way, the performance of fractional-NPLLs can approach that of integer-NPLLs. The SOC PLL in **Figure 1.4** takes advantage of Moore's Law to integrate a24-bit modulator, allowing the output frequency increment to be 0.06 ppm or smaller—an extremely fine resolution.

1.8.4 Advances in PLL quality

Beginning in the early '90s, IC designers began to incorporate passive inductors into ICs fabricated in generic CMOS-logic processes [9]. The Inductors have lower Q (quality) factorsthan do discrete components or similar inductors in an IC process tailored for RF.For decades, ICs have included capacitors in many forms, including gate-oxide,polysilicon-to-polysilicon, and metal-to-metal devices. The use of integrated inductors along with capacitors to form completely integrated LC (inductor/capacitor) VCOs greatly boosts performance(**Figure 1.5**). For a given fixed power level, LC VCOs typically outperform ring oscillators by 20 dB.

The LC-oscillator circuit predates ICtechnology. However, the integration of LC oscillators had been problematic until only the last 10 to 15 years.The first problem had to do with the inductor

itself. In process nodes larger than 0.25 microns, it was uncommon to have more than three metal layers,and the typical interconnect metal was aluminum.

Inductors in this process had relatively high series resistance,resulting in a low Q factor. The limited number of metal layers also meant that the inductor was physically close to the silicon surface. This situation in turn meant that these inductors had significant parasitic capacitance and hence allowed self-resonant frequency.

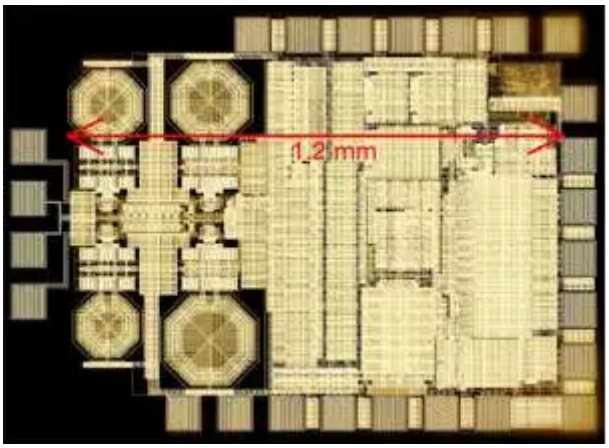


Figure 1.5 Integrated inductors have changed the appearance and performance of monolithic PLLs

The desire to integrate more gates has driven two advances in CMOS-processing technology, enabling the integration of practical inductors in genericCMOS-logic processes. The first, the use of CMP (chemical-mechanical polishing),makes each layer in the interconnect stack more planar, allowing for many stacked metal layers. In 180-nm technology, which debuted in the late 1990s, the use of six metal layers became common. Recent process technologies at 65 nm and smaller allow for 10 or more metal layers. The increase in metal layers allows designers to put the inductors in the top metal layers, far above the silicon surface, reducing the parasitic capacitance and increasing the self-resonant frequency. The second advance, the use of copper interconnect, allows for lower series resistance and a higher Q factor because copper interconnect has a lower resistance than aluminum.

The next problem related to the integration of inductors involved the relationship between inductance, oscillation frequency, and tank impedance:

$$\sqrt{L/C}\ The\ oscillation\ frequency\ is\ proportional\ to\ 1/\sqrt{L \times C}\ If\ capacitance\ is\ constant$$

A 2-GHz oscillator requires an inductor that is only 25% the size of a 1-GHz oscillator. As CMOStechnologies have advanced, higher frequencies have become possible,allowing smaller inductors. Hence, it has become economical to design and manufacture ICs with on-die inductors.
The performance of LC oscillators in integrated PLLs allows designers to choose integrated PLLs for applications with demanding phase noise, such asSONET (synchronous-optical-network)data transmission and cellular communication, which often require less than 1 psec of long-term jitter.Other advances in circuit design and process technology have allowed the integration of entire RF transceivers.

1.8.5 Current, future work

A current area of interest in PLLs is the digital PLL. Digital PLLs have a digital loop filter rather than an analog loop filter. The biggest advantage of a digital loop filter over an analog loop filter is size **(Figure 1.6)**. For analog PLLs, the sizeof the loop filter is a strong function of the PLL's bandwidth. For high-bandwidthPLLs, the loop filter consumes approximately 50% of the PLL area. For Low-bandwidth PLLs, the loop filter can become a large percentage of the PLL area. Even worse, a low-bandwidth analog PLL may require an external loop filter consuming valuable I/O pins and PCB area. In Contrast, as process technology advances, the area taken by addersand registers of a digital loop filter becomes steadily less important.

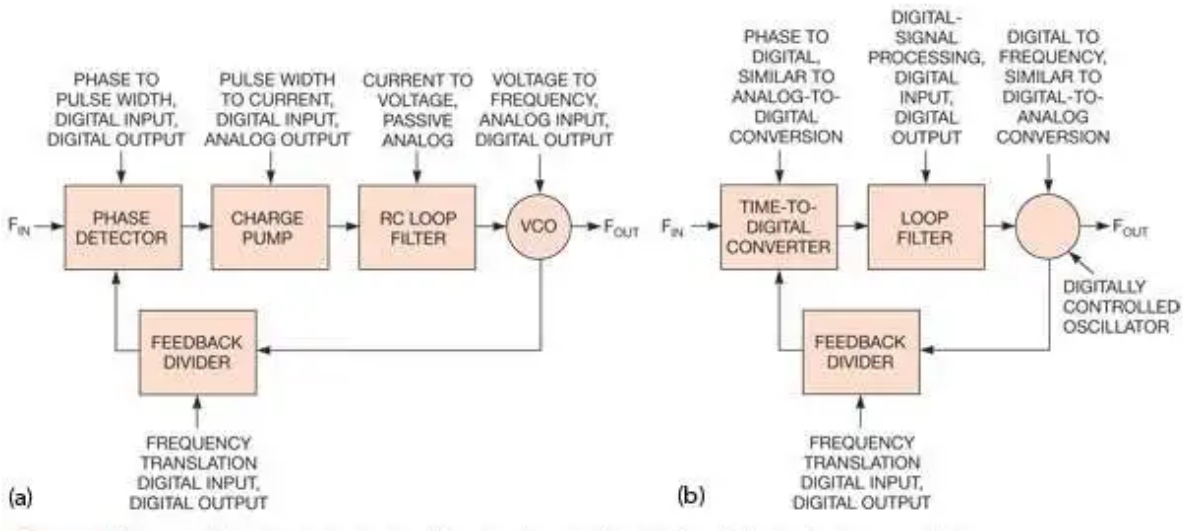


Figure 1.6 Analog PLLs (a) may be significantly larger than their digital counterparts (b).

In digital PLL,these designs require perhaps as much analog design as would a PLL using an analog loop filter. The analog PLL has two main analog design tasks.The charge pump and loop filter first convert PWM signals from the digital phase detector to current pulses and, inturn, to an analog control voltage. TheVCO then produces a frequency proportional to the analog tuning voltage.

The digital PLL replaces the digital phase detector of the analog loop by a phase-to-digital converter or time-to-digital converter. Think of this block as a sort of ADC but with an analog quantity that is phase or time rather than voltage. A DCO (digitally controlled oscillator) then replaces the VCO in the analog loop. This circuit is a type of DAC in which the analog quantity is frequency rather than voltage. So Digital-PLL design still has many challenging analog aspects.

Besides an area advantage, the digital loop filter also enjoys a noise advantage when scaling. The voltage noise on the analog loop filter scales as:

$\sqrt{KT/C}$,where k is the Boltzmann's constant, T is the absolute temperature, and C is the loop filter's capacitance.

If a design requires the noise to be a factor of two lower, capacitance must increase by four times. With the digital loop filter, the quantization noise scales as 0.5N, where N is the number of bits. To reduce the noise by a factor of two, a designer needs to add only a bit. A designer can easily make

the quantization noise in the digital loop filter negligible for little cost in area. However, this action pushes the problem of noise onto the time-to-digital converter and the DCO. Designinga time-to-digital converter and a DCOwith a large number of effective bits is still a significant challenge.

1.8.6 Uses for smaller PLLs

Advances in both circuit design and process technology have allowed SOCsto integrate more PLLs of various types.Besides frequency synthesis, several other applications of PLLs have become important. The integration of PLL forms one of the keys to serial chip-to-chip communication. This type of communication requires a SERDES circuitpair. Serial chip-to-chip communication has many benefits, most notably the reduction in IC area, because thePLL and SERDES are typically smaller than the set of parallel I/Os, and in PCB complexity because the serial links require fewer traces. The last decade has seen the emergence of standards such as PCIe (Peripheral ComponentInterconnect Express), XAUI (10-Gbps Attachment-unit interface), SATA (serial-advanced-technology attachment),USB (Universal Serial Bus) 3.0, andGbE (gigabit Ethernet), among others.

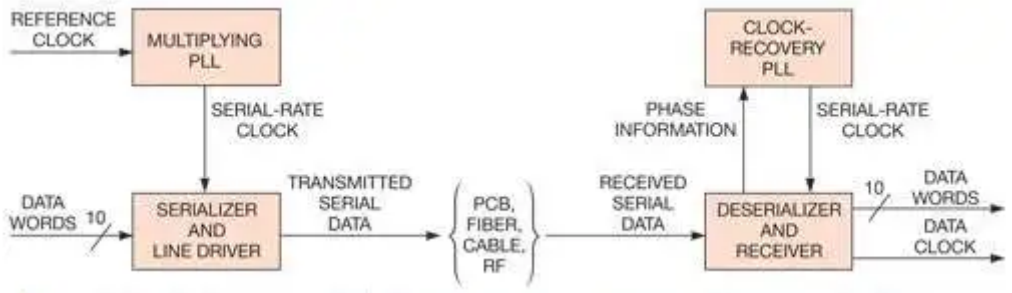


Figure 1.7 Serial chip-to–chip links have become important applications of PLLs

Both the serializer and the deserializer functions rely on PLLs to generate their clocks. The serializer requires a low-jitter, frequency-multiplying PLLfor the transmitter. The PLL multiplies the parallel-rate clock frequency up to the serial rate. A multiplication by 10 to the parallel rate is common. The Serializer PLL typically specifies less than 1% rms (root mean square) of the clock period for long-term jitter—for example, 1 psec rms at 10 Gbps.

The receiver requires a CDR (clock- and data-recovery) circuit, a type ofPLL that locks to incoming data rather than to a clock. CDR circuits have for decades found use in optical communication.However, CDR circuits have only in the last decade become small enough and low enough in power to make integrated SERDES practical.

One of the first integrated CDR circuits was part of a 2.488-Gbps chipset whose developers fabricated it in gallium-arsenide and silicon-bipolar technology [10]. It used an external loop filter and an external transmission line for the resonator in the VCO. In the 20 years since this integratedCDR debuted, the same advancements that have helped other types ofPLLs have helped CDRs to shrink in power and area. Standard CMOS-logic processes integrate CDRs that require no external components and consume much less than 1 mm2 of chip area.

The miniaturization of PLLs opens many other types of applications to these devices. Common examples include deskewing PLLs, which align the clock at the end of a clock tree with an input clock, and multiphase PLLs, which generate four to 32 output clocks with equally spaced phases and find use in RFreceivers and multichannel CDR circuits.

PLLs have come a long way since the emergence in the 1970s of monolithicPLLs. Much of this advancement has come from the improvements in process technology. Further improvements in performance have come from innovative circuit-design techniques.With these developments, PLLs have become versatile and essential building blocks. Modern SOCs, such as multimedia processors, contain eight to 20PLLs performing diverse functions. As Technology advances, PLLs will find use in even more applications.

The technological trajectory of PLLs has seen significant refinements, particularly in enhancing performance metrics like lock time, stability, and phase noise. Best, in Phase-Locked Loops: Design, Simulation, and Applications [1], chronicles these advancements, discussing various design strategies that have evolved over decades. Best also provides insight into the simulation and practical application of PLLs, highlighting the iterative nature of technological enhancement in response to growing demands for more robust communication systems. Early implementations of PLLs have been foundational in setting the stage for complex modulation systems. Historically, PLLs have facilitated significant advancements in communication systems, marking critical transitions in how signals are modulated, demodulated, and synchronized. Scholarly works from the late 20th century [2] provide a comprehensive overview of these foundational implementations, highlighting their impact on the efficiency and reliability of early communication systems.

Chapter 2: Design And Dimensioning Of The VHF PLL

2.1 Introduction

The intricate journey of frequency modulation (FM) technology, especially within the domain of communication systems, underscores a relentless quest for clarity, reliability, and efficiency in data transmission. Central to this evolutionary path is the development and refinement of the Phase-Locked Loop (PLL), a mechanism pivotal in maintaining signal synchronization and integrity. This chapter aims to present and size the different circuits that enable the practical realization of the various roles and functions required for effective FM communication. By meticulously analyzing the theoretical underpinnings, including the relevant equations and simulation profiles, this review seeks to encapsulate the pivotal discussions and scholarly contributions that have shaped the field.

2.2 Brief analysis of fm modulation

Frequency modulation (FM) modulation is a method of encoding information onto a carrier wave by varying the frequency of the wave according to the amplitude of the modulating signal. Here's a brief analysis:

2.2.1 Advantages:

- **Improved Noise Immunity:** FM modulation offers better noise immunity compared to amplitude modulation (AM), making it more resilient to interference.
- **Higher Quality Audio:** FM signals are less susceptible to amplitude variations, resulting in higher quality audio transmission, particularly for broadcasting music and speech.
- **Bandwidth Efficiency:** FM signals can carry more information within a given bandwidth compared to AM signals, allowing for the transmission of multiple channels simultaneously.
- **Signal-to-Noise Ratio:** FM modulation maintains a constant signal-to-noise ratio across the transmission range, ensuring consistent signal quality.

2.2.2 Disadvantages:

- **Complexity:** FM modulation and demodulation circuits are more complex compared to AM systems, requiring additional components and precise tuning.
- **Frequency Bandwidth:** FM signals require a wider frequency bandwidth compared to AM signals, which can lead to spectrum congestion in densely populated areas.
- **Nonlinear Distortion:** FM signals are sensitive to nonlinear distortions in the transmission medium, which can affect signal quality.
- **Cost:** Implementing FM modulation systems, particularly in broadcasting applications, can be more expensive due to the need for specialized equipment and infrastructure.

Overall, FM modulation offers several advantages in terms of signal quality and noise immunity, particularly in applications where high-fidelity audio transmission is crucial. However, it also comes with challenges related to complexity, bandwidth requirements, and cost, which must be considered when designing and implementing FM communication systems.

2.3 Foundational Concepts of PLLs

The concept of the PLL has been foundational in communication systems, providing mechanisms for frequency stabilization and synchronization essential for reliable signal transmission. Gardner's seminal work, Phaselock Techniques [2], offers a comprehensive exploration of the basic operational principles of PLLs, including the roles and functions of their core components such as phase detectors, loop filters, and voltage-controlled oscillators. Gardner explains how these components interact to achieve system stability and accuracy, which is crucial for understanding both traditional and modern implementations of PLLs.

The concept of the Phase-Locked Loop (PLL) stands as a cornerstone in communication systems, facilitating frequency stabilization and synchronization crucial for dependable signal transmission. Gardner's seminal work, "Phaselock Techniques," provides an insightful exploration into the foundational principles underpinning PLLs. At the heart of a PLL lie three indispensable components: (1) a phase detector (PD), (2) a loop filter (LF), and (3) a voltage-controlled oscillator (VCO) (see Figure 2.1). The PD compares the phase of an input signal against that of the VCO, generating an error signal indicative of the phase difference. Subsequently, the LF filters this error signal, adjusting the VCO frequency to minimize phase deviation. When locked, the PLL ensures the VCO frequency aligns precisely with that of the input signal, though some residual phase error may persist. Excessive phase error causes loss of lock.

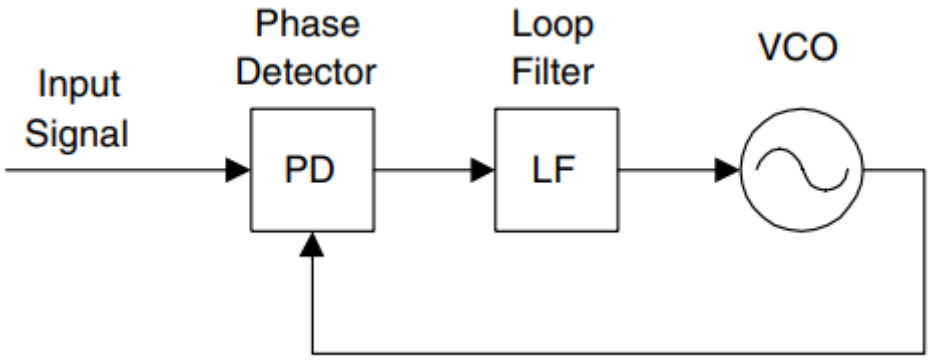


Figure 2.1 Basic phaselock loop.

Gardner delves into crucial properties of PLLs, emphasizing bandwidth and linearity. Bandwidth, a critical property of phaselock loops, distinguishes between narrow and wide bandwidth PLLs, each serving distinct purposes. Narrow bandwidth PLLs address scenarios where the input signal, possibly distorted by noise, requires faithful reproduction. Here, a local oscillator closely matches the signal's expected frequency, enabling the phase detector to compare waveforms and determine instantaneous phase differences. By averaging these errors over time, the PLL filters noise, ultimately aligning the oscillator's frequency and phase with the clean signal. This characteristic makes PLLs akin to filters, proficient in passing signals while rejecting noise. Conversely, wide bandwidth PLLs stabilize oscillators with erratic frequencies, counteracting fluctuations through rapid response mechanisms. Although inherently nonlinear, most PLLs are analyzed using linear techniques in their locked state, leveraging the simplicity and effectiveness of such methods for analysis and initial design.

2.3.1 Choice and Characteristics of Phase Detector

2.3.1.1 Analog Phase Detectors:

- Cost-effective for VHF ranges
- **AD834 UHF multiplier:** operates up to 500 MHz, full-scale error of 0.5%

2.3.1.2 AD834 Multiplier Key Features:

- Converts voltage inputs to current before multiplication (To reduce noise and drift)
- Ensures accurate performance for input voltages up to 1V, input voltages above 1V may cause distortion due to clipping

2.3.2 Preliminary Loop Filter (1st Order RC Low-Pass Filter)

Improves PLL performance by removing high-frequency noise

2.3.3 Varicap Diode in VCO

- Uses MV2201 varicap diode for frequency control via voltage adjustments
- Accurate capacitance measurement at different voltages
- Ensures precise tuning and stability of the VCO

2.3.4 VCO Design

2.3.4.1 Transistor Selection

- BFR92A transistor: suitable for VHF band.

2.3.4.2 Hartley Oscillator Configuration

- Ensures positive feedback for stable oscillations
- Focus on accurate admittance calculations
- Design achieves necessary frequency range and stability for PLL operation

2.3.4.3 VHF Amplifier Key Points

- **Optimization:** Achieved through parametric sweep simulation
- **Frequency Range:** 97.872 MHz to 98.128 MHz (linear response for small variations in the bias voltage (Vbias), the VCO maintains a linear frequency response. This ensures precise control over the output frequency.)
- **Stability:** Ensures stable VCO operation with minimal distortion

2.4 DESIGN AND DIMENSIONING OF THE VHF PLL

2.4.1 Overview of received FM information

The baseband of the information to be modulated in FM reaches 15KHz, contrary to the AM or baseband is truncated at 4.5kHz. in our case, the maximum frequency is further extended up to F=22KHz normalized. Taking the standard frequency excursion, ΔF=75KHz, the modulation index is:

$$\delta = \frac{\Delta F}{F} = \frac{75}{22} = 3.4$$

The index being greater than 1, indicates that the FM obtained is broadband (wind 9 spectral lines for a mod N). With a frequency band occupied by the FM modulated signal: B= 2(ΔF+F)= 194kHz a frequency range of 88 MHz to 108 MHz, is available for FM transmitters. By setting a carrier frequency in the middle of this range, i.e. FP=98 MHz, the instantaneous frequency of the modulated signal becomes:

$$f(t) = fp \pm \frac{B}{2} = 98\,MHz \pm 97kHz = [97,903MHz\ to\ 98,097MHz]$$

As a first simulation step, we prefer to start with a simple case of narrow-band FM modulation. In this case, we adopt a fairly high modulating frequency in order to easily follow the spectrum obtained in simulation. Therefore a sinusoidal modulation in FM, or F= 128kHz. The modulation index must be less than 1:

$$\delta = \frac{75}{128} = 0,586 \quad \text{.....(2.1)}$$

Indicating a spectrum mainly carrying 2 lines between the carrier frequency; and occupying a band:

$$B = 2(\delta + 1)\,\Delta F \simeq 2\Delta F = 150kHz \quad \text{.....(2.2)}$$

This case fixes the variation interval of the instantaneous frequency of the modulating signal:

$$f(t) = 98\,MHz \pm 75kHz = [97,925\,MHz\ to\ 98,075\,MHz] \quad \text{.....(2.3)}$$

In the case of sinusoidal FM modulation, the LF information is written:

$$V_0 = E_0 Cos\Omega t \quad if \quad \Omega = 2\pi f = 2\pi \times 128KHz \quad \text{.....(2.4)}$$

The FM modulated signal can be written as:

$$V_1 = E_1 Cos(\omega pt + \varphi_1)\ if:$$
$$\left\{\varphi_1 = \delta\, cos\,\Omega t\ with\ \delta = 0.586\ and\ \omega_p = 2\pi \times 98MHZ\right\} \quad \text{.....(2.5)}$$

On receiver, the PLL presents at the output of its VCO when it is locked:

$$V2 = E2\cos(WPt + \varphi 2)\ ou\ \varphi 2 = \delta \sin(\Omega t + \frac{\pi}{2}) = \delta \cos \Omega t \ldots\ldots\ldots\ldots\ldots\ldots(2.6)$$

At the output of the multiplier circuit then as a phase detector, we will have:

$$Vd = K\,V1\,V2 = \frac{K\,E1\,E2}{2}[\cos(2\omega_p t + \varphi 1 + \varphi 2) + \cos(\varphi 1 - \varphi 2)] \ldots\ldots\ldots\ldots\ldots\ldots(2.7)$$

.

The useful term of (7) is kept by filtering:

$$V_F = U\cos(\varphi 1 - \varphi 2) = U\cos\{\delta[\sin \Omega t - \cos \Omega t]\} \ldots\ldots\ldots\ldots\ldots\ldots(2.8)$$

Either :

$$VF = U\cos[\sqrt{2}\,\delta \sin(\Omega t - \frac{\pi}{4})] = U\sum_{-\infty}^{+\infty} Jn\,(\delta\sqrt{2})\cos[n(\Omega t - \frac{\pi}{4})] \ldots\ldots\ldots\ldots\ldots(2.9)$$

If Jn (..) represent the Bessel functions of the 1st kind of order n and argument $\delta\sqrt{2}$

As FM is narrow band ($\delta < 1$), two lines mainly ± F constant around 0.
This is the demodulated baseband.
with n=1; the expression (2.9):

$$VF = \frac{\delta U}{\sqrt{2}}\cos(\Omega t - \pi\backslash 4) \ldots\ldots\ldots\ldots\ldots\ldots(2.10)$$

which represents the LF information of expression (2.4) phase shifted by $\frac{\pi}{4}$.

2.4.2 Choice and characteristic of phase detector:

The best phase detectors are digital in nature but the operating frequency range is VHF, an analog phase detector is more economical. This is a multiplier circuit operating on VHF. Initially, the choice was based on the AD835 VHF multiplier whose minimum band length announced by the manufacturer is 150MHz. However, the stance of the Gain, within -0.1 dB, does not exceed 15MHz, which can cause an intolerable variation in the voltage product carried out at 100MHz. The four-quadrant UHF multiplier, AD834, easily meets the need for a product between VHF signals. It is a monolithic circuit operating up to 500MHz from differential voltage inputs and whose typical full-scale error is 0.5%. More details are given in the following subtitle.

Or the product between two sinusoidal voltages, ensured by a multiplier of gain $K(v^{-1})$:

$$K.E_1\cos(\omega_1 t + \varphi_1) \times E_2\cos(\omega_1 t + \varphi_1) = \frac{KE1E2}{2} \times$$
$$\{\cos[(\omega_1 + \omega_2)t + \varphi 1 + \varphi 2] + \cos[(\omega_1 - \omega_2)t + \varphi 1 - \varphi 2]\} \ldots\ldots\ldots\ldots\ldots(2.11)$$

The band filter of the PLL being low pass in nature, eliminates the HF component provided by the phase detector and retains the useful one of lower frequency. The PLL then undertakes to ensure equality in the input frequencies, before moving on to that between phases.

Therefore be the useful term of the phase detector:

$$U_d = \frac{KE1E2}{2} cos(\varphi 1 - \varphi 2) = K_d \times cos\,\Delta\varphi \quad \text{(2.12)}$$

$$with\ Kd\ detector\ sensitivity\ V\backslash rd$$

It is a sinusoidal characteristic, therefore non-linear, but becomes linear for a low U_d value or well. for small phase difference Δφ around $\frac{\pi}{2}$. In other words, the phase comparator based on a multiplier ensures within a PLL, a phase quadrature between its two input voltages at equal frequencies in steady state.

2.4.2.1 AD834 multiplier:

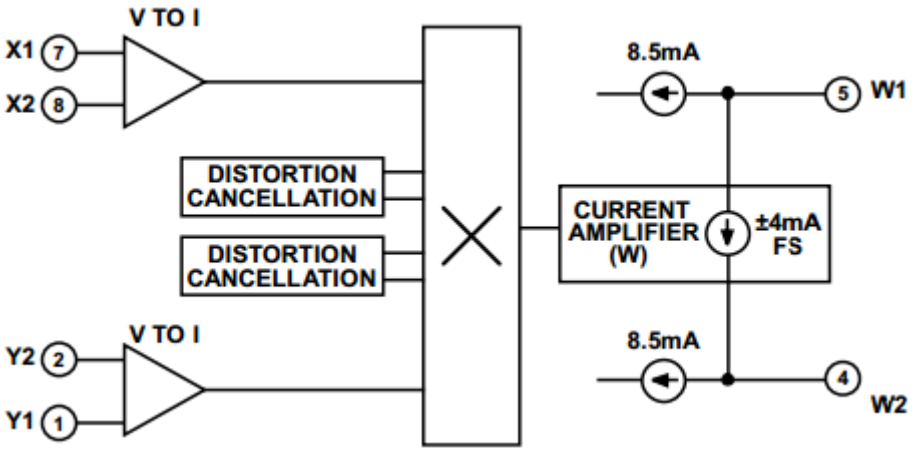


Figure 2.2: AD834 functional block diagram

Figure 2.2 illustrates the AD834 circuit block diagram, where the two differential inputs X and Y undergo voltage-to-current conversion before being applied on the multiplication block; the output W is based on my current differential pair based on transistors with open collectors.

The transfer function is adjusted again so that the output differential current is ±4mA. So that (X=Y= ±1V).

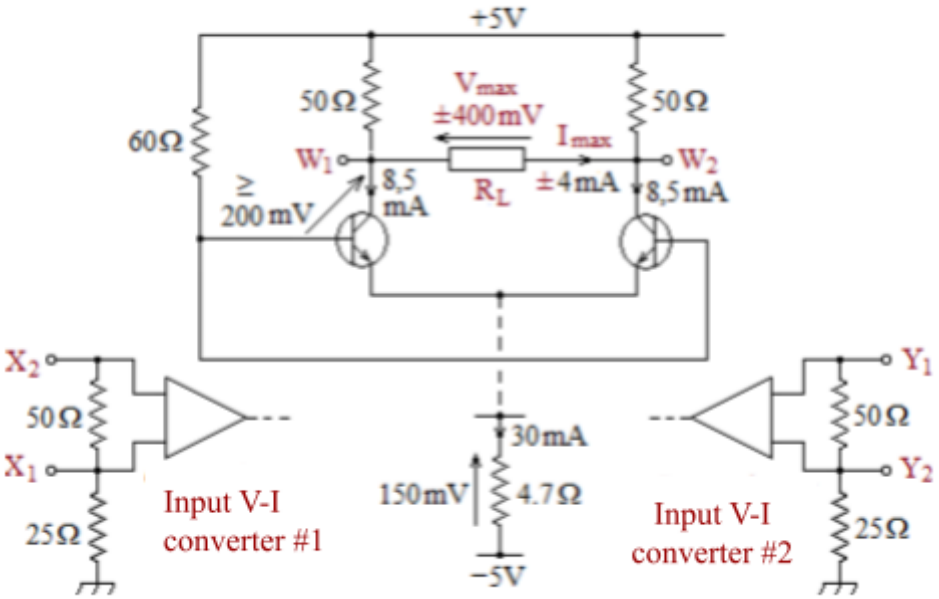


Figure 2.3: Converter VI for input 1 or 2

Figure 2.3 shows the output current while the two input voltages: X=X1-X2 and Y=Y1-Y2, are positive.

The collector currents at rest are typically 8.5mA and are a ±5V supply, to find resistors of 50 Ω. The manufacturer recommends the insertion of a terminal resistor of 50Ω at each differential input. The bias input current being typically 45µA, this generates a significant offset voltage unless it is compensated by the insertion of another resistor of 25Ω before connecting the ground to inputs X1 and Y2. The input impedances, X1 and Y1 therefore become normalized to 75Ω.

Input voltages are first converted to current, to reduce noise and drift. Distortion elimination circuits are also used, which further improves circuit performance. In order to avoid saturation of the output transistors, the collector voltages must be greater than or equal to 200mV relative to those of the bases. Using 50Ohm resistors at both collectors, this gives a differential output voltage of plus or minus 400mV full scale, and simply placing a 60Ohm resistor is sufficient to ensure proper polarization of the two bases. The 4.7Ohm resistor limits a current of approximately 30mA, destined for the negative power supply of the circuit. The important thing is to note that the clipping of the differential output signal is written when for each output transistor is checked:

- During the alternation smaller than 0 of its output at

$$I_{c\,max} = 8.5 + 4 = 12.5\ mA,\ on\ a\ V_{CB\,min} \geq 200\,mV$$

$$either\ V_{c\,min} - V_{B\,max} = (5V - 50 \times 12.5m) - (5V - 60 \times I_{DC}) \geq 200mV$$

$$or\ I_{DC} \geq 13.75\,mA \quad \text{.....(2.13)}$$

- During the alternation greater than 0 of its output:

$$I_{c\,min} = 8.5 - 4 = 4.5\,mA,\ we\ have\ V_{CB\,max} \geq 200mV$$

$$either\ V_{c\,max} - V_{B\,min} = (5V - 50 \times 4.5m) - (5V - 60 \times I_{DC}) \geq 200\,mV$$

$$or\ I_{DC} \geq 7.083mA \quad \text{.....(2.14)}$$

Thus, the most severe condition that must be respected is:

$$I_{DC} \geq 13.75\,mA.$$

Furthermore, the manufacturer of the AD834 circuit informs that the output also becomes clipped when the input voltage reaches $\pm\ 1.3V$, and that the nominal full-scale attempt is limited to $\pm\ 1V$. It is said, the transfer function of circuit AD834 we the expression of its output W in fact of the two inputs X and Y is given by:

- Current output: $W = \frac{XY}{(1V)^2} \times 4\,mA$ .....(2.15)
- Voltage output: $W' = W \times 250Ohm = \frac{XY}{1V}$.....(2.16)

2.4.2.2 preliminary loop filter

The loop filter is essential for two reasons: for the first, it must eliminate the HF Parasite term from the multiplier and keep the useful LF term, expression 1. For this, it must be low pass - the second reason is to 'make a possible correction to the response of the PLL, in order to improve its static and dynamic performances - This last step will be addressed at the end of the design of the PLL, once all the data is gathered. Here, the creation of a simple 1st order RC filter followed by a differential stage acting as a Balun circuit (balanced-unbalanced output).

The data from the differential output of the circuit of Figure 2.3, gives the nominal load resistance:

$$R_L = \frac{400\,mV}{4\,mA} = 100Ohm$$

This resistor is followed by a Capacitor C in series, so as to produce a first order low pass filter whose Cutoff frequency Fc is set slightly lower than the modulating frequency.

$$F = 128KHz.\ So\ then:$$

$$F_C = 100KHz = \frac{1}{2\pi R_L C} \Rightarrow C \simeq 16nF \quad \text{.....(2.17)}$$

Figure 2.4 brings together the phase detector, the RC filter, and the differential amplifier ensuring an asymmetrical output relative to ground. Slight modifications are made to certain resistors of the phase detector, in order to ensure intensities at the collectors as well as other values mentioned in Figure 2.3 - the three capacitors of the RC filter are arranged so as to ensure an AC connection to the LM324 type difference amplifier.

Noting V_{c1}, the output voltage of capacitor C and VC_3, that of capacitor C_3, figure 2.4, the output of the op-amp LF is expressed for equal resistances:

$$V_S = \frac{R_4}{R_1} \times \frac{R_1 + R_2}{R_3 + R_4} v_{C1} - \frac{R_2}{R_1} v_{C3} = v_{C1} - v_{C3} = v_{C2} \quad \text{.....(2.18)}$$

Thus the differential trend at the bases of C_2, is found at the output of the op-amp in relation to ground. This voltage therefore represents the useful filtered voltage of the phase detector, given by expression (2.5). For input voltages of the phase detector, fixed at 1V and at the same frequency 98MHZ, a “phi” phase shift is however provided between them.

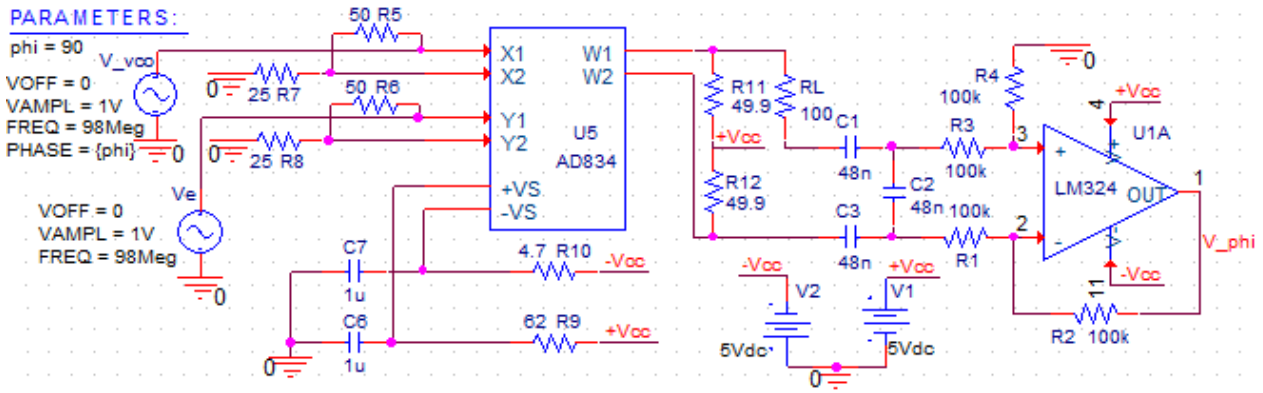


Figure 2.4: Phase detector assembly + RC filter + differential amplifier

The circuit in Figure 2.4 is subjected to the following simulation profile:

- Type of analysis: time domain, from 8us to 8.1us, in steps of 0.1ns.
- Parametric sweep: global parameter = phi, linear type of sweep from 0 to 180° in increments of 2.

The measurement therefore begins from 8us, which is the response time of the detector estimated to be:

$$5RC = 5 \times 100\Omega \times 16nF = 8us.$$

The phase characteristic obtained from the detector, and provided in Figure 2.5, vanishes for (phi = 90°)(residual voltage measured at -159uV).

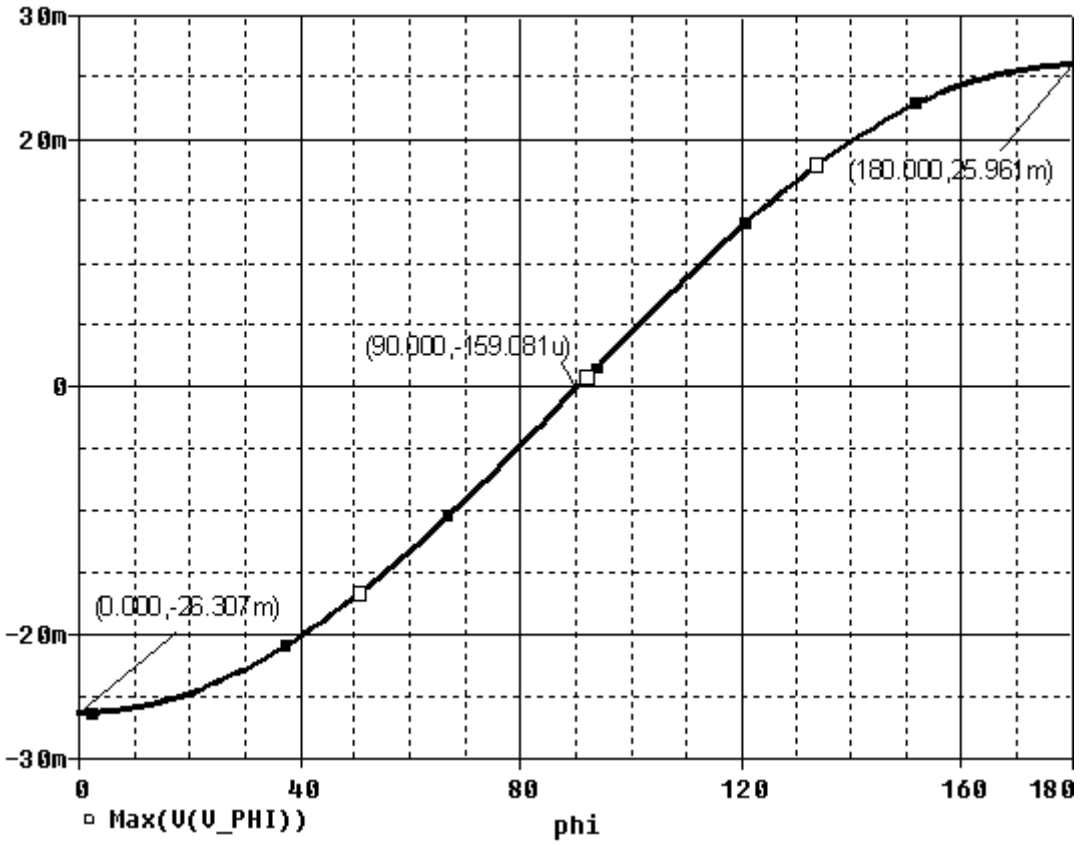


Figure 2.5: Phase characteristic of the AD834 multiplier

We measure a sensitivity of the detector, equal to:

$$Kd = 26mV\ /Degree\ 1.5V/rd.$$

The Negative Sign being due to the inverse shape of the cosine of the characteristic obtained - In the time domain, the amp output voltage is found low; 9uV peak to peak.

The input impedance of the AD834 being fixed at 75Ω, the VCO must be capable of powering this load and consequently, also becomes greedy current. It is therefore wise to provide safety amplification at the output of the differential amplifier associated with the RC filter. This is a common collector buffer stage of the classic 2N2222 type;

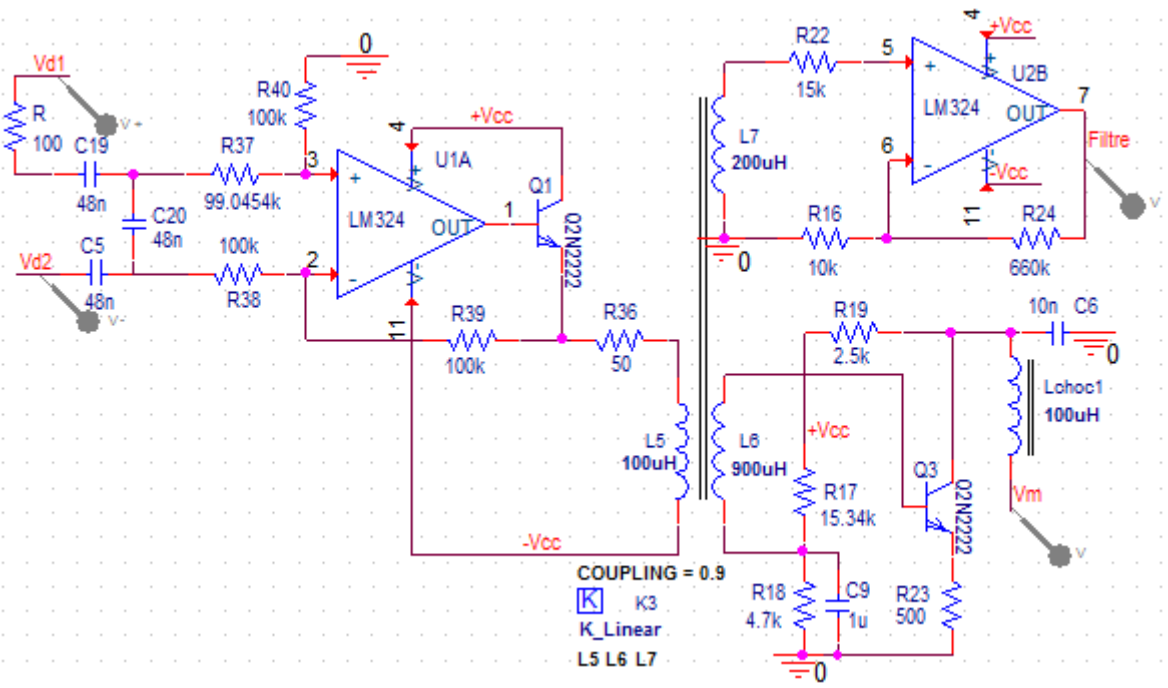


Figure 2.6: Interface between phase detector and VCO with filter output to LF circuitry

To pioneer the processing of alternating signals from the differential amplifier, the load at the transmitter of the 2N2222 is linked to - Vcc - This load is essentially inductive, therefore to a transformer ensuring an AC connection with two separate amplifiers. An amplifier based on a 2nd amp-rp of the LM32A, ensures the output of the demodulated signal intended for the UI LF of the receiving station its voltage gain is fixed at:

$$1 + \frac{660\,K}{10K} = 67$$

The theoretical polarization resistance is:

$$R_{22} = \frac{R_{16}}{R_{24}} = 9.9K\Omega$$

Affinity to 15K by simulation in order to compensate for the offset current. The other amplifier based on a 2N2222 transistor, is a VCO driver with a voltage amplification of $-\frac{2{,}5K}{0{,}5K} = -5$ the filtered signal. A positive direct voltage to the VCO in order to poralise the varicap diodes. On the other hand, it prohibits the passage of the VHF frequency from VCO to the driver, of which a 10nF capacitor is provided as a 2nd order low pass filter with a cutoff frequency:

$$\frac{\frac{1}{jc\omega}}{jl\omega+\frac{1}{jc\omega}} = \frac{1}{1-LC\omega^2} \rightarrow fc = \frac{1}{2\Pi\sqrt{LC}} = \frac{1}{2\Pi\sqrt{0{,}1\,m\,.\,10\,m}} = 159KHz \quad \text{.....(2.19)}$$

This value is chosen in order to allow the LF modulating signal with its DC component to pass through, without, however, allowing the VHF signal from the VCO to pass in the other direction. As the VCO rest frequency is chosen in the middle of the alliance VHF band at standard

FM-90MHZ, the polarization voltage of the VCO varicap diodes is also chosen at half of VCC, i.e. +2,5 V. An collector of the driver, we therefore have:

$VC = 2,5\,V\ and\ IC = 1mA\ fixed$, Which gives $RC = 2,5\,K\Omega$, and
$VCE0 = 2V\ for\ RE = 0,5\,K\Omega$. By the way $RB = \frac{R17}{R18}$ as resistance from the base.
The basic voltage is:

$$\frac{R_{18}}{R_{17}+R_{18}}VCC = \frac{R_B}{R_{17}}VCC \Rightarrow \frac{R_B}{R_{17}} = \frac{1,1}{5} = 0,22 \quad \text{.....(2.20)}$$

The current stability factor of the basic polarization is written:

$$\text{If: } \frac{RB+RE}{RE+\frac{RB}{\beta}} \rightarrow RB = \frac{(SI-1)RE}{1-\frac{SI}{\beta}} = 3,23\,K\Omega \quad \text{.....(2.21)}$$

For $\beta \simeq 100$ and $SI = 7$ selected. From (2.20):

$R17 = \frac{R_B}{0,22} = 14,66K$ adjusted by simulation to 15,34KΩ

And :

$R18 = \frac{R_{17}.R_B}{R_{17}-R_{18}} = 4,14K$ adjusted by simulation to 4,7KΩ

In dynamics, the 10nF capacitance associated with the shock choke causes the gain of the driver calculated to be -5. The person in charge collects from coming $\frac{RC}{\frac{1}{CW}}$ this capacitance at the frequency LF, 128KHz, Becomes:

$$\frac{1}{C\omega} = \frac{1}{2\Pi.10\,n.128K} = 124\Omega$$

The load on the collector coming from $\frac{RC}{\frac{1}{C\omega}} = 0,12\Omega$, hence the voltage gain movement of the driver:

$$GV = \frac{0,12}{0,5} = -0,24$$

This attenuation is partially composed of a secondary taken nine times higher than the primary, set at 100µH.

2.4.3 Varicap diode Characteristics:

The VCO being part of the PLL, requires an element fixing its frequency using a control voltage among the simple means used in practice, is the use of a Varicap diode. The selected MV 2201 diode gives the EVAL library of Pspice, and is analyzed from a measuring bench illustrated in Figure 2.7. In addition to its reverse bias, the diode is subjected to an oscillation at a frequency of 98MHZ with an amplitude that does not compromise its blocked state. Thus, its capacitance characteristic as a function of the reverse bias voltage is one of the conditions closest to its

operation within the VHF oscillator. The measuring bench also makes it possible to trace the theoretical characteristic of the diode, obtained by manual adjustment of the construction parameters established in its transfer function:

$$CD = \frac{Cjo}{(1+\frac{Vr}{Vj})^{M}} \quad \text{.....(2.22)}$$

Where:

$Cjo \Rightarrow$ *is the junction capacity at rest*

$Vj \Rightarrow$ *is the direct senile voltage of the junction*

$Vr \Rightarrow$ *is the reverse polarization voltage of the junction*

$M \Rightarrow$ *is a real exponent*

This transfer function is programmed in an ABM element.

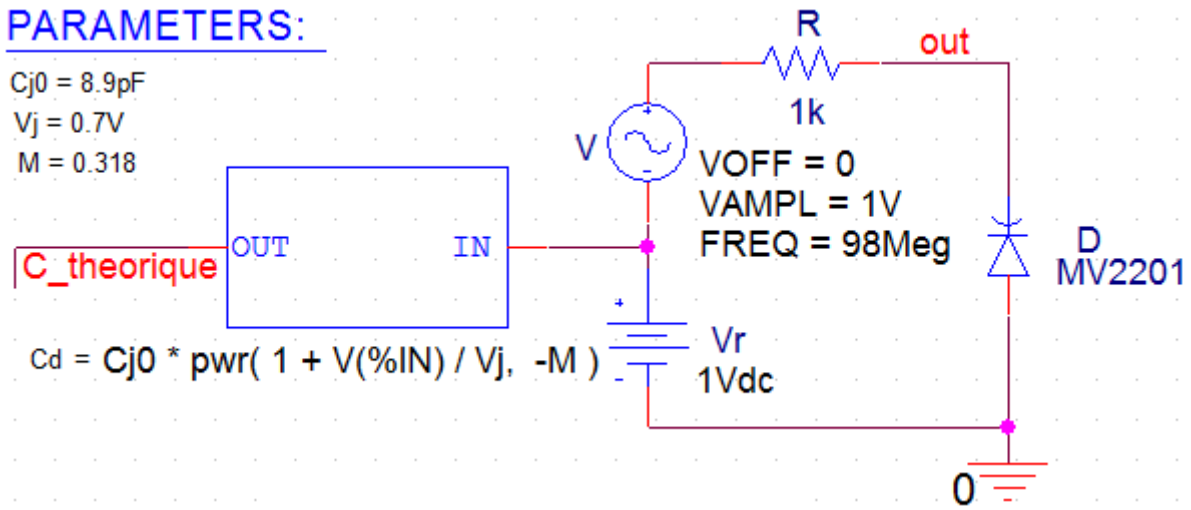


Figure 2.7: Measuring bench for the characteristic of the varicap diode

Which is driven by the polarization voltage Vc, providing the characteristic of the diode at the theoretical output. After adjustment, Figure 2.8 shows a perfect superposition of the theoretical and measured characteristics of the diode, therefore with a maximum difference of 0.3pF. Adjusting the parameters gives:

$$Cjo = 8,9\,pF\,;\; Vj = 0,7V\,;\; M = 0,318\,;\; therefore\ a\ measure\ of:$$
$$Cd = 5,49\,pF\ to\ Vr = 2,5V$$

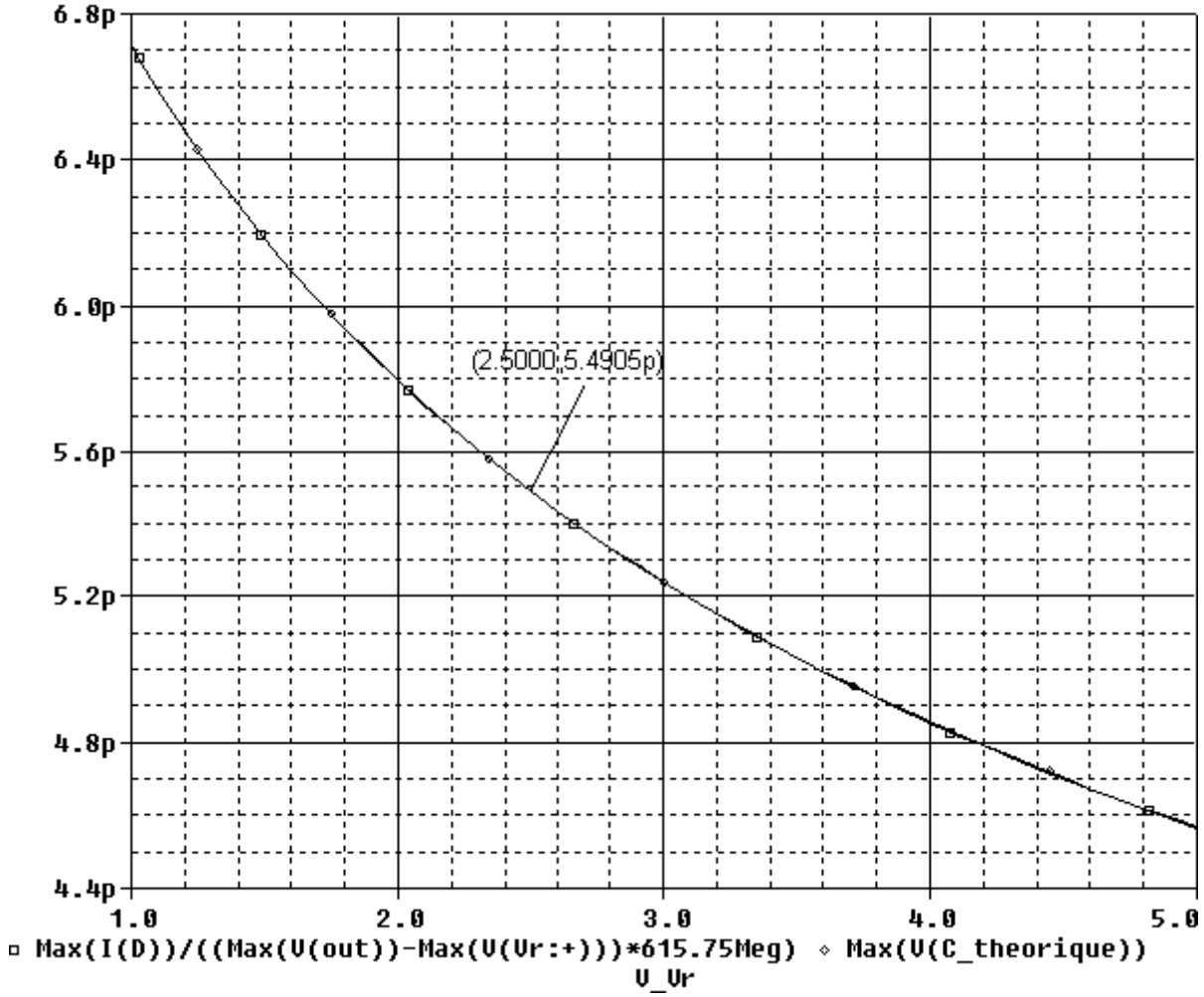


Figure 2.8: Theoretical and measured superposition characteristics of the varicap diode

2.4.4 Design of the VCO:

To increase the frequency, an appropriate transistor must be chosen, the broadband BFR92A transistor easily covers the VHF band. Of these graphic measurements, only one point is of interest, this one at the frequency of 100MHZ. Thus, these bridges are transferred to a real Smith chart from which the approximate values of the reduced Sij could be noted:

$$\begin{aligned} S11 &= 1{,}1 - j1{,}2 \\ S12 &= 0{,}02\, e^{j\,70^\circ} = (6{,}84 + j18{,}79).10^{-3} \\ S21 &= 2{,}3\, e^{j140^\circ} = -17{,}62 + j14{,}78 \\ S22 &= 2{,}6 - j52 \end{aligned} \qquad \text{……..(2.23)}$$

$$With:\ \Delta S = S11\,S22 - S12\,S21 = -59,14 - j60,1$$

In VHF, a short circuit can be made and not an open circuit because of parasitic capacitances. Thus, the representation of the transistor using the admittance parameters is admissible, since these parameters are defined relative to short circuits. The transistor having to be adapted to the input impedance Z0 = 75Ω of the phase detectors, the conversion of Sij to Y_{ij} gives:

$$Y_{11} = \frac{1}{Z0}\,\frac{1+S22-S11-\Delta S}{1+S11+S22+\Delta S} = g_{11} + j\,x_{11} \Rightarrow$$

$$g_{11} = -3,72\,.\,10^{-3}SI \qquad x_{11} = 5,47.\,10^{-3}SI$$

$$Y_{12} = \frac{1}{Z0}\,\frac{-2\,S12}{1+S11+S22+\Delta S} = g_{12} + j\,x_{12} \Rightarrow$$

$$g12 = 4,22\,.\,10^{-6}SI \qquad x12 = 4,19.\,10^{-7}SI \quad \text{.....(2.24)}$$

$$Y_{21} = \frac{1}{Z0}\,\frac{-2\,S21}{1+S11+S22+\Delta S} = g_{21} + j\,x_{21} \Rightarrow$$

$$g_{21} = -1,2\,.\,10-3 \quad x_{21} = -4,73.\,10-3SI$$

$$Y_{22} = \frac{1}{Z0}\,\frac{1+S11-S22-\Delta S}{1+S11+S22+\Delta S} = g_{22} + j\,x_{22} \Rightarrow$$

$$g_{22} = -13,3\,.\,10^{-3}SI \qquad x_{22} = 5,12\,.\,10^{-4}SI$$

Quartz at 100MHZ exists, but that at 98MHZ does not. Our VHF oscillator will therefore have an RC circuit whose configuration is that of Hartley with a transformer. The equivalent dynamic circuit of such an oscillator is shown in Figure 2.9 with its decomposition into two quadrupoles in parallel, separating the real parts from the imaginary parts of the components.

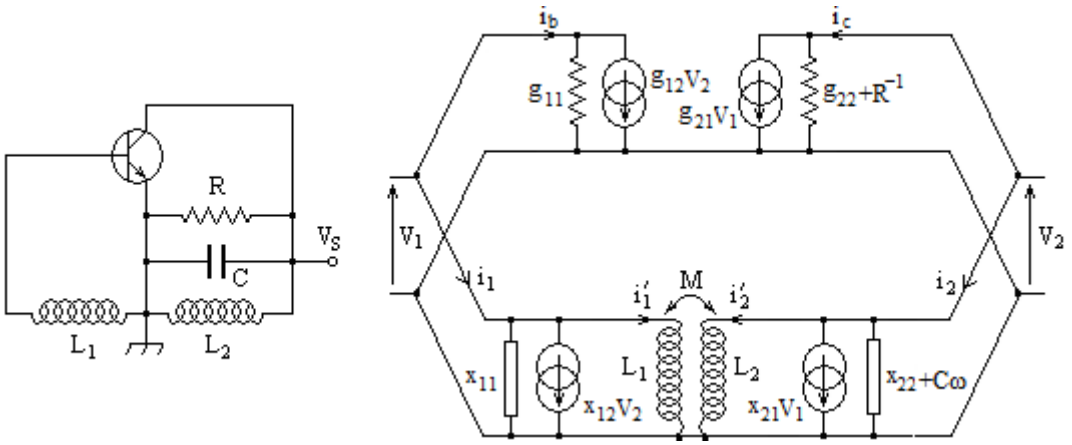


Figure 2.9: Equivalent diagram in the dynamics of the oscillator and its decomposition into quadrupoles

The loop resulting from this association ensures a positive reaction necessary for the maintenance of the oscillations. The transformer must be a phase inverter, in order to compensate for the phase inversion caused by the transistor mounted as a common emitter and the phase rotation at 2 was thus accomplished. The oscillation condition of the circuit dictates that the determinant of its admittance matrix must be zero. Let's start by determining the admittance matrix of each quadrupole.

Real quadrupole:

$$\begin{pmatrix} i_b \\ i_c \end{pmatrix} = \begin{pmatrix} g_{11} & g_{12} \\ g_{21} & g_{22}+R^{-1} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \quad \text{.....(2.25)}$$

Imaginary quadrupole: Consider the mutual magnetic induction between primary L1 and secondary L2 of the transformer, M = $\alpha\sqrt{L_1 L_2}$ where α is the magnetic coupling coefficient, $\alpha \ll 1$:

$$V_1 = j L_1 \omega i_1^{'} + j M \omega i_2^{'} \; and \; V_2 = j L_2 \omega i_{22}^{'} + j M \omega \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.26)$$

With:

$$i_1^{'} = i_1 - j (x_{11} V_1 + x_{12} V_2) \; and \; i2^{'} = i2 - j [x_{21} V_1 + (x_{22} + c\omega) V_2] \ldots\ldots (2.27)$$

We place (2.27) in (2.26):

$$j L_1 \omega i_1 + jM \omega i_2 = A V_1 - B V_2 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.28)$$
$$jM \omega i_1 + j L_2 \omega i_2 = - D V_1 + E V_2$$

Or:

$$A = 1 - L_1 \omega x_{11} + M \omega i_{21}$$
$$B = L_1 \omega x_{12} + M \omega (x_{22} + c\omega) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.29)$$
$$D = L_2 \omega x_{21} + M \omega x_{11}$$
$$E = 1 - L_2 \omega (x_{22} + c\omega) - M \omega x_{12}$$

We divide the 1st equation of (2.28) by jMw and its 2nd equation by $jL_2\omega$, in order to isolate i_2:

$$\frac{L_1}{M} i_1 + i_2 = \frac{A V_1 - B V_2}{jM\omega} \; and \; \frac{M}{L_2} i_1 + i_2 = \frac{-D V_1 + E V_2}{jL_2\omega} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.30)$$

Whose difference gives:

$$(\frac{L_1}{M} - \frac{M}{L_2}) i_1 = (\frac{A}{jM\omega} + \frac{D}{jL_2\omega}) V_1 - (\frac{B}{jM\omega} + \frac{E}{jL_2\omega}) V_2 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.31)$$

Similarly, this time we divide the 1st equation of (2.28) by $jL_1\omega$ and its 2nd equation by $jM\omega$, in order to isolate i_1:

$$i_1 + \frac{M}{L_1} i_2 = \frac{A V_1 - B V_2}{jL_1\omega} \; and \; i_1 + \frac{L_2}{M} i_2 = \frac{-D V_1 + E V_2}{jM\omega} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.32)$$

Whose difference gives:

$$(\frac{M}{L_1} - \frac{L_2}{M})i2 = ((\frac{A}{jL_1\omega} - \frac{D}{jM\omega})V_1 - (\frac{B}{jL_1\omega}\frac{E}{jM\omega})V_2 \text{.....(2.33)}$$

On the other hand we have:

$$\frac{L_1}{M} - \frac{M}{L_2} = \frac{L_1}{M}(1-\alpha^2) \; and \; \frac{M}{L_1} - \frac{L_2}{M} = \frac{L_2}{M}(\alpha^2 - 1) \text{.....(2.34)}$$

(2.31) and (2.33) then gives:

$$\begin{pmatrix} i_1 \\ i_2 \end{pmatrix} = \frac{M}{J\omega(1-\alpha^2)} \begin{pmatrix} \left(\frac{A}{M}+\frac{D}{L_2}\right)\frac{1}{L_1(1-\alpha^3)} & -\left(\frac{B}{M}+\frac{E}{L_2}\right)\frac{1}{L_1} \\ -\left(\frac{A}{L_1}+\frac{D}{M}\right)\frac{1}{L_2} & +\left(\frac{B}{L_1}+\frac{E}{M}\right)\frac{1}{L_2} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \text{.....(2.35)}$$

Total Currents $i_1 + i_b$ and $i_2 + i_c$ debited respectively Without V1 and V2, used to determine the admittance matrix of the oscillator.

$$\begin{pmatrix} i_1 + i_b \\ i_2 + i_c \end{pmatrix} = \begin{bmatrix} Y_{tot} \end{bmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \text{.....(2.36)}$$

These currents must cancel for a closed system on an oscillator, which implies a zero determinant of the matrix Y_{tot}.

$$Note\ well:\ (y) \times (v) = (i) = (0) \rightarrow (v) = (y^{-1})(i) = \frac{1}{det(y)}\ com\,(y^T).(i) = \frac{(0)}{(0)}$$

Undetermined state.

For $(v) = 0$. Athus, the matrix (y) is singular, i.e. it is square with zero determinant.

The total admittance matrix of the circuit is the sum of the admittance matrices of the two total quadrupoles, (2.25) and (2.35); both:

$$Y_{tot} = \begin{pmatrix} g_{11} + \frac{M}{JL_1\omega(1-\alpha^2)}\left(\frac{A}{M}+\frac{D}{L_2}\right) & g_{12} - \frac{M}{JL_1\omega(1-\alpha^2)}\left(\frac{B}{M}+\frac{E}{L_2}\right) \\ g_{21} - \frac{M}{JL_2\omega(1-\alpha^2)}\left(\frac{A}{L_1}+\frac{D}{M}\right) & g_{22} + R^{-1} + \frac{M}{JL_2\omega(1-\alpha^2)}\left(\frac{B}{L_1}+\frac{E}{M}\right) \end{pmatrix} \text{.....(2.37)}$$

With zero determinant and separating the real parts from the imaginary parts. Two equations emanating after development:

$$A\left[Mg_{12} + L_2(g_{22} + R^{-1})\right] + B(Mg_{11} + L_2g_{21}) + D\left[L_1g_{12} + M(g_{22} + R^{-1})\right] + E(Mg_{21} + L_1g_{11}) = 0 \quad \text{(2.38)}$$

$$\left[g_{11}(g_{22} + R^{-1}) - g_{12}g_{21}\right]L_1L_2\omega^2(1 - \alpha^2) + BD - AE = 0 \quad \text{(2.39)}$$

Which become respectively with (2.29) and:

$$\Delta x = x_{11}x_{22} - x_{12}x_{21}$$
$$\Delta g = g_{11}g_{22} - g_{12}g_{21}$$

$$L_1L_2cg_{11}(1 - \alpha^2)\omega^2 + L_1L_2(1 - \alpha^2)\left[g_{11}x_{22} + (g_{22} + R^{-1})x_{11} - g_{12}x_{21} - g_{21}x_{12}\right]\omega - L_1g_{11} - M(g_{12} + g_{21}) - L_2(g_{22} + R^{-1}) = 0 \quad \text{(2.40)}$$

$$L_1L_2cx_{11}(1 - \alpha^2)\omega^3 - \left[c + L_1(1 - \alpha^2)(g_{11}R^{-1} + \Delta g - \Delta x)\right]L_2\omega^2 - (L_1x_{11} + L_2x_{22} + Mx_{12} + Mx_{21})\omega + 1 = 0 \quad \text{(2.41)}$$

By Posing this time,

$$A = L_1L_2cg_{11}(1 - \alpha^2)$$
$$B = L_1L_2(1 - \alpha^2)\left[g_{11}x_{22} + (g_{22} + R^{-1})x_{11} - g_{12}x_{21} - g_{21}x_{12}\right] \quad \text{(2.42)}$$
$$D = -\left[L_1g_{11} + M(g_{12} + g_{12}) + L_2(g_{22} + R^{-1})\right]$$

And like $-4AD \gg 0 \Rightarrow \sqrt{B^2 - 4AD} \gg B$ the oscillation frequency and the solution of (2.40):

$$\omega_0 = \frac{\sqrt{B^2 - 4AD} - B}{2A} = 2\pi \times 98MHZ \quad \text{(2.43)}$$

By injecting (2.43) into (2.41), as Parameters g_{ij} and x_{ij}. Of the transistor are determined, it remains to choose certain elements of the oscillator, such as:

$$\alpha = 0.9 \; and \; C = 12pF + 2.75pF \; (where: \frac{CD}{2} = 2.75pF)$$

See figure 2.10.

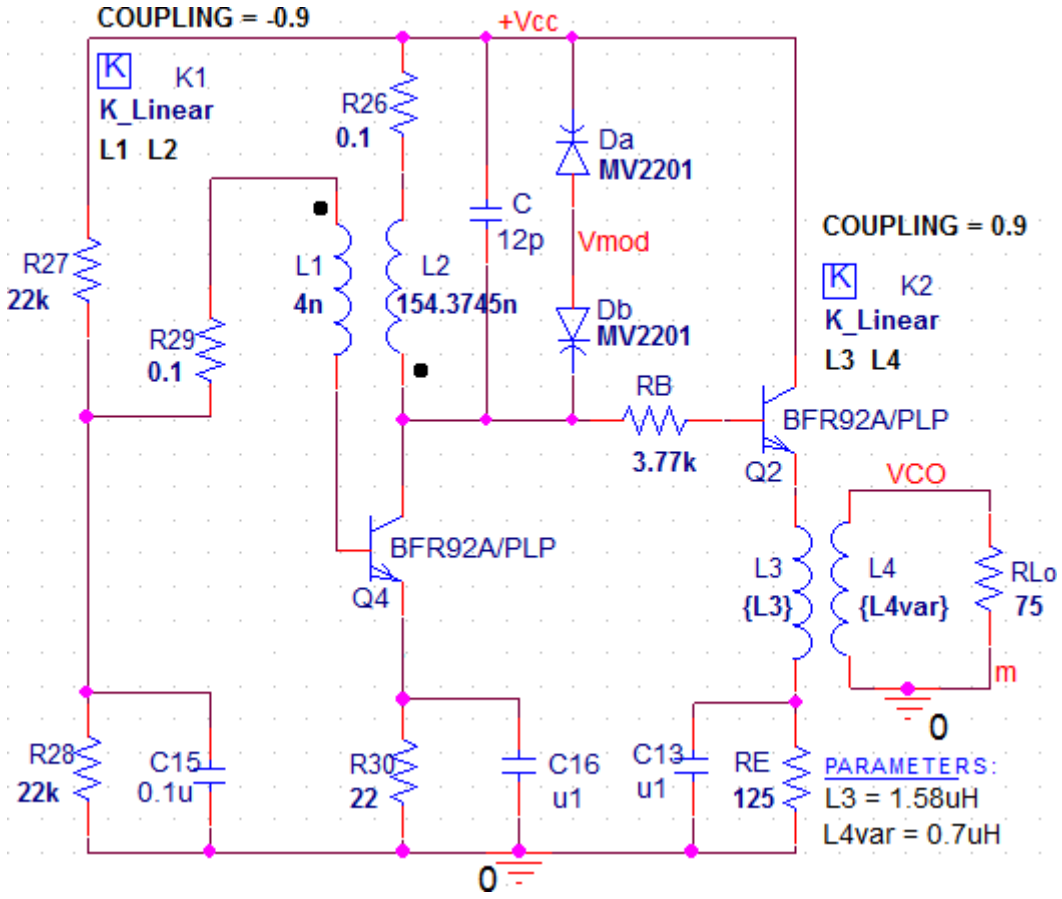


Figure 2.10: VCO circuit + buffer stage adapted to 75Ω

The resistances are to be calculated from the static study, started below. To remain unknown to me, only the bolts L_1 and L_2 of the transformer. These two unknowns are to be determined from the two equations (2.41) and (2.43) where all the other parameters of these two equations are known.

The characteristics of the BFR92A transistor are taken from its data sheet:

$$I_{Cmax} = 25mA;\ B = 90;\ P_{tot} = 300mw\ ;\ transition\ frequency\ F_T = 1GHZ;$$
$$noise\ figure\ F = 2,1\ db\ .$$

The oscillator being called to deliver high currents, the quiescent collector current is set at:

$$I_{C0} = 12mA \simeq \frac{I_{Cmax}}{2}.\ Which\ gives\ a\ base\ current\ I_{B0} = 12mA/90 = 133mA$$
$$Or\ a\ basic\ voltage\ V_{B0} = 1V$$

The transmitter voltage is:

$$R_E = \frac{300mV}{(12+0.133)mZ} = 24.7\Omega$$

Adjusted by simulation to 22Ω, figure 2.10, because B_0 is measured at 83.6 instead of 90. Thérenin's model applied to the input polarization circuit, allows us to write:

$$E_{th} = R_B I_{B0} + R_{B0} \; or \; R_B$$

Is the equivalent resistance of the basic part made up of the resistances R_{27} and R_{28}.

Either: $R_{27} = R_{28} = 2R_B$ and $E_{th} = \frac{V_{cc}}{2} = 2.5V$

So we have: $R_B = \frac{2.5V-1V}{133mA} = 11K\Omega \rightarrow R_{27} = R_{28} = 22K\Omega$

The constraint of the VCO is to ensure at the level of its load (75 at the input of the Phase detector), a nominal voltage of amplitude 1V, or a load current $\frac{1V}{75\Omega} \simeq 13mA$ of amplitude, which are necessary to do this. It is prudent to provide a buffer stage guaranteeing current amplification and which is developed below.

2.4.4.1 VHF amplifier:

The transistor then still being of the BFR92A type, the chosen collected current is close to I_{Cmax}.

$$Either: \; I_{C0} = 24mA, \; VE_0 = 3V$$

$$From \; where:$$

$$I_{B0} = \frac{24mA}{38.6} = 287mA \; and \; R_E = \frac{3V}{24mA} = 125\Omega$$

The base voltage becomes:

$$VB_0 = 3V + 0,8V = 3,8V$$

Which allows the calculation of the basic resistance:

$$R_B = \frac{V_{CC}-V_{B0}}{I_{B0}} = \frac{5V-3,8V}{0.287mA} = 4,18K\Omega$$

Adjusted by simulation to $3.77K\Omega$, figure 2.10, because of B_0 which changes with I_{C0} and which is measured here at 78 instead of 83.6. In dynamics, we tolerate an emitter charge arriving at $1K\Omega$; developed by the primary of the transformer, figure 2.10.

$$L_3\omega_0 = 1K\Omega \Rightarrow L_3 = \frac{1K\Omega}{2\pi \times 98MHZ} \simeq 1.58uH$$

The load 75Ω of VCO being wired to secondary L_4, The latter is initially taken as a variable in order to optimize its value. For this is in addition to the indications given in the temporal analysis starting the Simulation from 170us to 170.1us in steps of 0.1ns; the parametric sweep option is checked in order to mention the name "L4var" as a global parameter. The linear sweep type is selected, ranging from 0.1uH to 1uH in steps of 0.05uH; Figure 2.11.

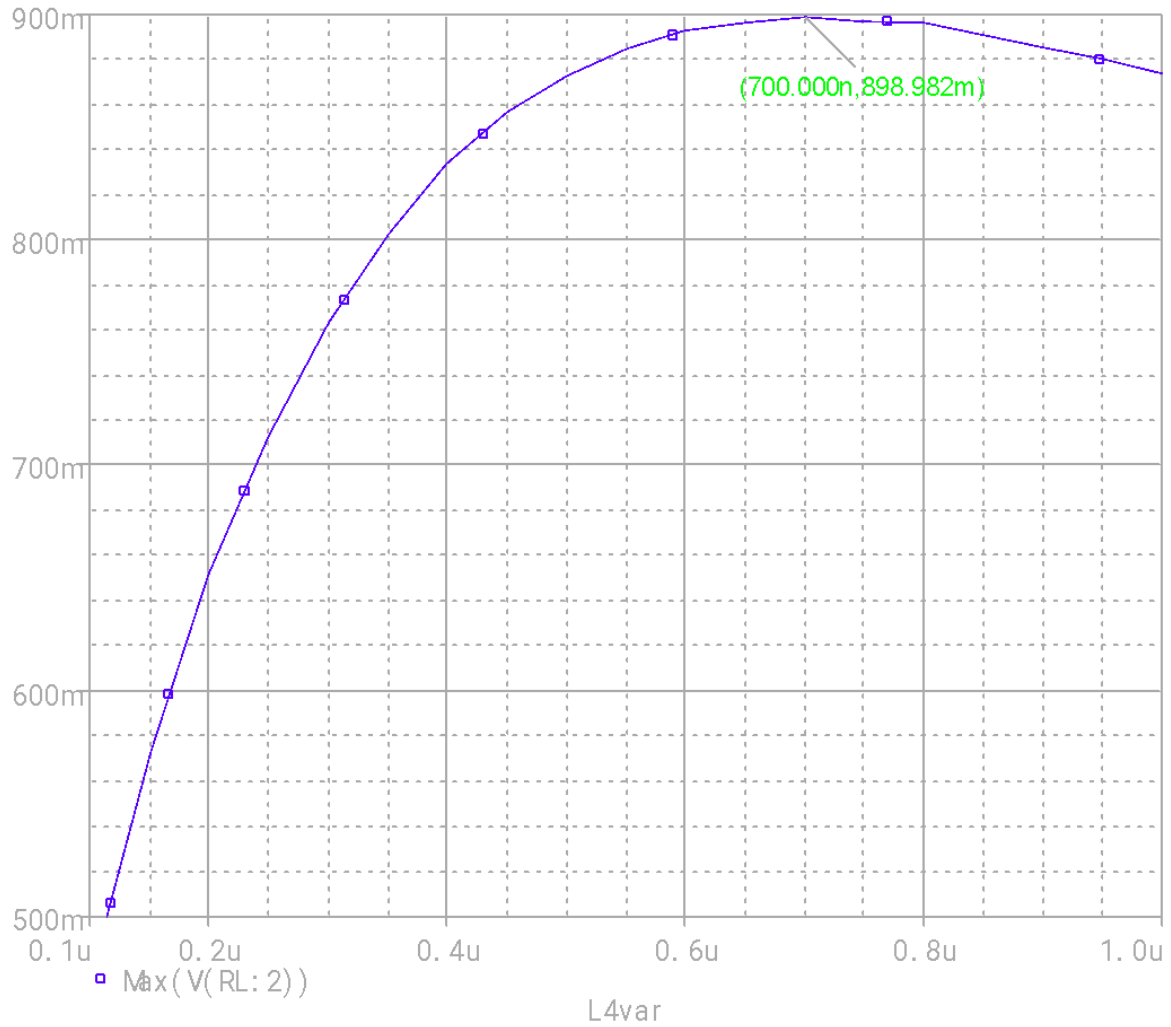


Figure 2.11: Measurement of the optimal value of the VHF amplifier transformer secondary

$L_4 = 0.7uH$ is the value of the secondary which ensures a maximum voltage amplitude equal to 0.9V at the input of the phase detector, at the input over impedance terminals normalized to 75. Going back to the transistor-oscillator, its dynamic load constituted by the VHF amplifier must be determined in order to be fixed, the resistance R in Figure 2.9. This resistance is included among many other parameters in the calculation of the oscillator frequency (2.43) and its maintenance condition (2.41). Calculating the transformer within the oscillator from these two equations promises to be tedious and this requires completing the VCO Design with the help of PSpice. Hence the values of the coils L_1 *and* L_1 of the VCO transformer, found by trial and error in Figure-2.10.

The VCO once completed, was subject to measurements shown in Figure 2.12.

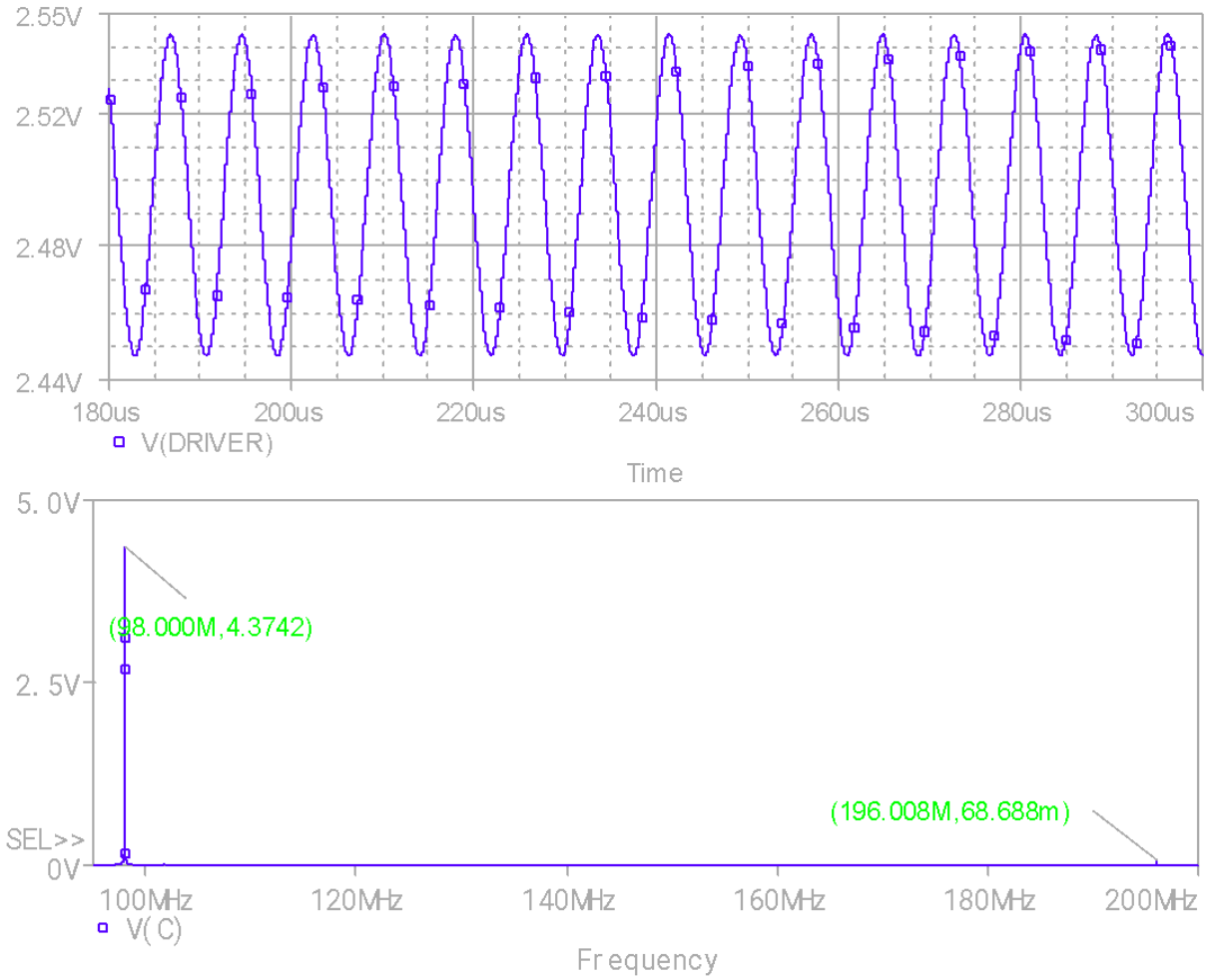


Figure 2.12: VCO quiescent signal and its spectrum

The Quiescent signal of the VCO measures in steady state at the frequency 98MHz, its frequency spectrum is associated with it where two lines appear. This is the fundamental of amplitude 4.4V at the frequency 98MHz and its 2nd harmonic of amplitude 69mV at double frequency 196MHz. The appearance of harmonics in the spectrum of the periodic signal provides information on the harmonic distortion which is measured over 10 harmonics and before 1.6%.

DC COMPONENT = 5.024108E+00

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	9.800E+07	5.150E+00	1.000E+00	-1.617E+01	0.000E+00
2	1.960E+08	6.906E-02	1.341E-02	-1.170E+02	-8.468E+01
3	2.940E+08	2.006E-02	3.895E-03	-6.812E+01	-1.962E+01
4	3.920E+08	1.239E-02	2.405E-03	2.361E+01	8.828E+01
5	4.900E+08	2.104E-02	4.086E-03	8.285E+01	1.637E+02
6	5.880E+08	2.530E-02	4.912E-03	1.242E+02	2.212E+02
7	6.860E+08	2.156E-02	4.186E-03	1.644E+02	2.776E+02
8	7.840E+08	1.126E-02	2.187E-03	-1.534E+02	-2.410E+01
9	8.820E+08	1.524E-03	2.958E-04	2.172E+00	1.477E+02
10	9.800E+08	9.660E-03	1.876E-03	8.999E+01	2.517E+02

TOTAL HARMONIC DISTORTION = 1.635517E+00 PERCENT

Figure 2.13: Table that shows distortion analysis of oscillation frequency up to 10 harmonics

If the load of the VCO is less important than the input impedance 75 of the phase detector, the alternating signal of the VCO would be less distorted. For example, for a 5K load the sinusoidal signal of the VCO on Quiescent was purer with harmonic distortion falling to 1.3%.

The 98MHz Quiescent frequency of the VCO is fixed using varicap diodes biased by the voltage source $V_{bias} = 2.5V$, and applied at point P between the anodes of the two diodes, figure 2.10.

To trace the voltage frequency characteristic of the VCO, the time simulation profile is shown from 100µs to 100.1µs in steps of 0.1ns. The parametric sweep option is checked, in order to indicate the voltage source V bias as the variable sounds a linear type of sweep from 0.1V to 3.5V in 0.1V increments. The characteristic obtained from the VCO indicated in figure 2.14. The frequency of the VCO as a function of the bias voltage V bias of the varicap diodes, is non-linear. But for a small variation in the established frequency of the modulating signal (6), ranging from 97.872MHz to 98.128MHz around the Quiescent frequency 98 MHz, the characteristic of the VCO is completely linear.

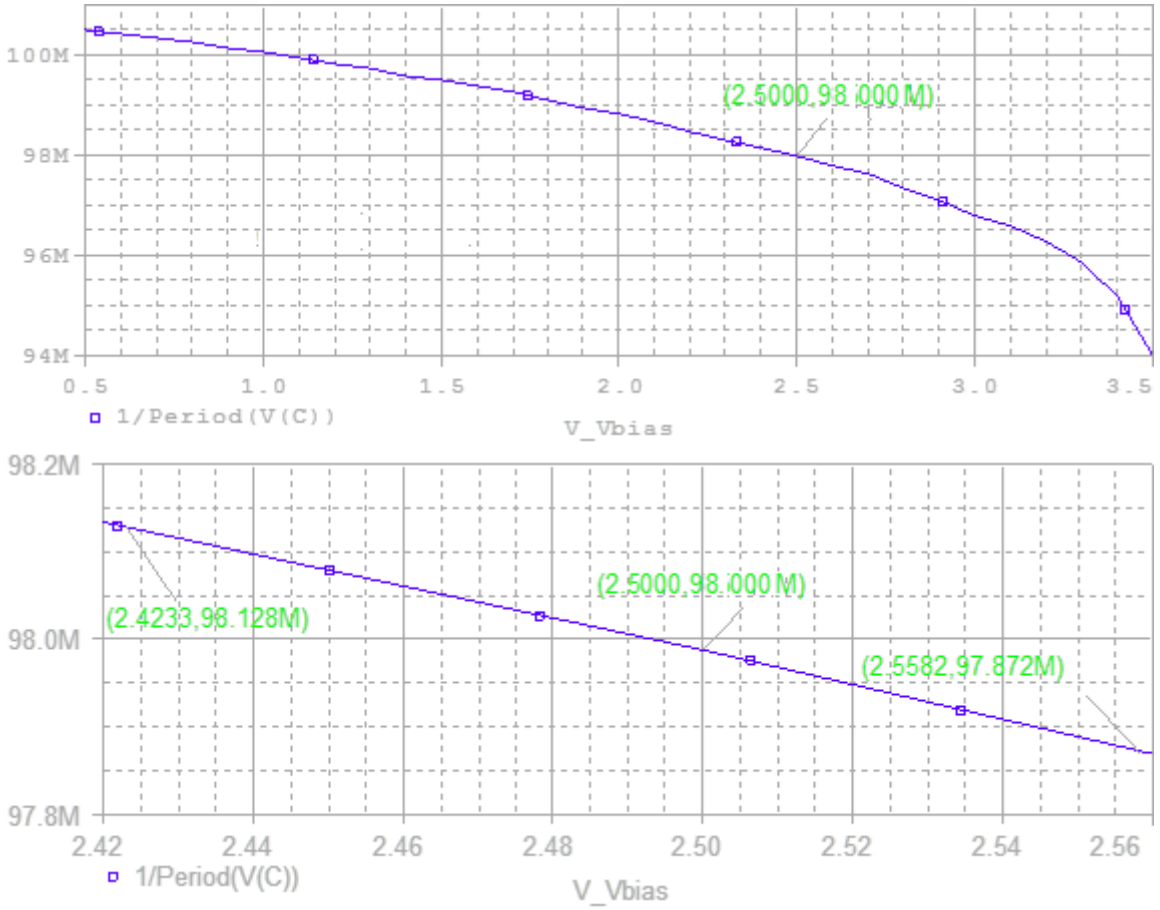


Figure 2.14: Frequency-voltage characteristic of the VCO (zoom at the bottom)

From this characteristic, the sensitivity of the VCO is derived:

$$K_0 = \frac{2\Pi . \Delta f}{\Delta V bias} = \frac{2\Pi(98,128-97,872)MHz}{(2,5582-2,4233)\,V} = 11,9 \times 10^6\, rd/vs \quad \text{.....(2.44)}$$

Figure 2.10 contains in addition to the VCO circuit and its VHF amplifier, a driver stage to control the VCO in frequency modulation. The modulating signal being fixed at 128MHz for narrow-band modulation, (4) and (5), the driver circuit is the same discussed and presented in figure 2.6. Its V_{MOD} output is to be applied in place of point P of the VCO circuit in Figure 2.10.

In steady state, the frequency modulated signal of the VCO by V_{MOD} or V_{driver} is illustrated in figure 2.15.

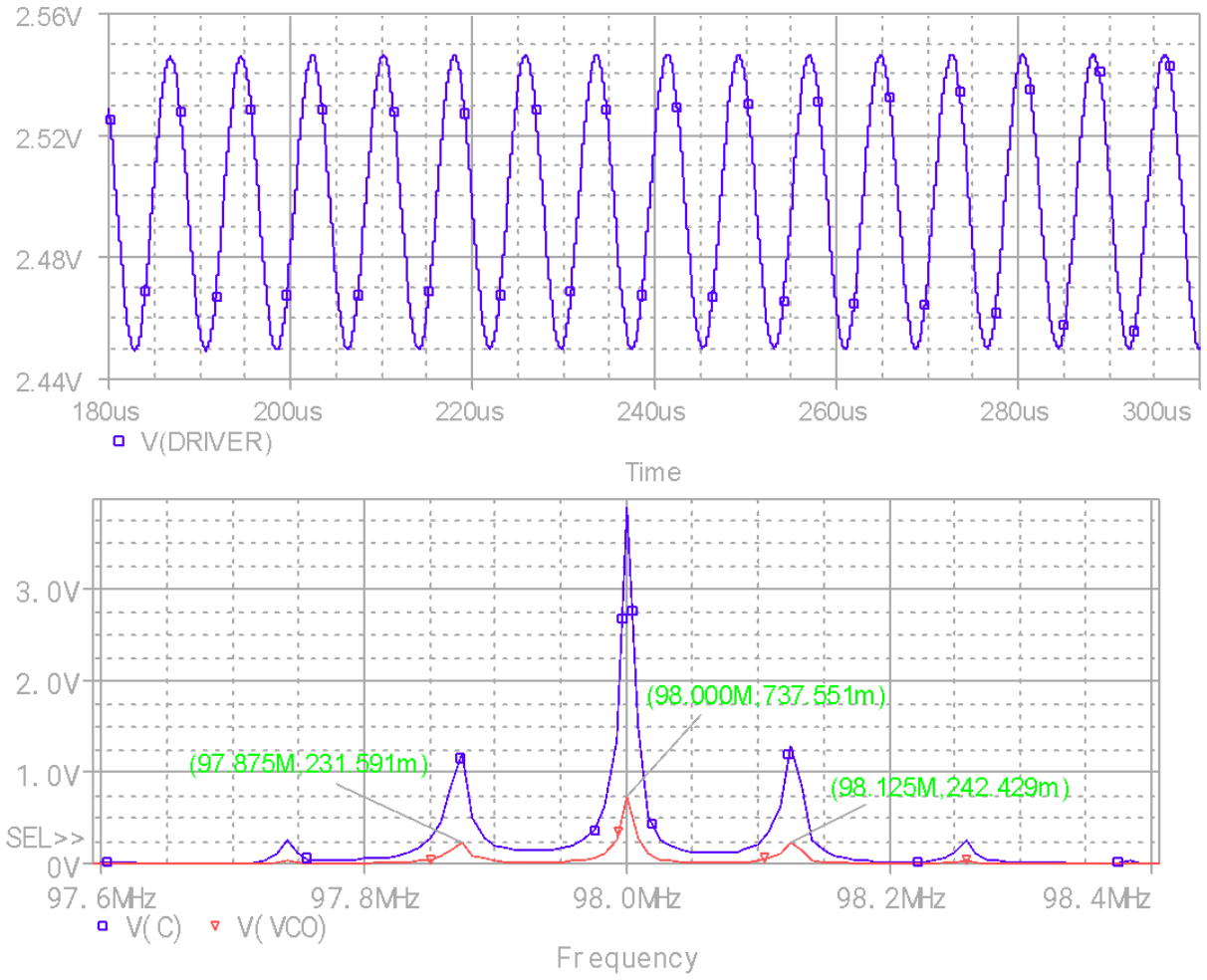


Figure 2.15: Driver signal and spectrum of narrow-band FM modulation at the transistor-oscillator collector and VCO load

The low voltage coming from the driver varies well around $V_{bias} = 2,5V$. The spectrum of the modulation or collector signals of the transistor-oscillator and across its 75Ohm load in Figure 2.10, are superimposed in Figure 2.15. The spectrum of narrow-band FM modulation is naturally reduced to two rays at ± 128KHz around the carrier, but as the index $\delta(4)$ is not really negligible compared to 1, two other lines considered weak are present at ±128KHz around the carrier.

The two main lines of the spectrum are mentioned at frequencies:

$$98M - 125K = 97.875MHz \; and \; 98M + 125K = 98.125KHz$$

Instead of 98M 128KHz in figure 2.15. This is a relatively short simulation time. A longer simulation time allows precise convergence on the expected frequencies of the two lines.

2.5 Homodyne Receivers

2.5.1 Rx - Frequency Conversion

Rx - Frequency Conversion [14]
Frequency of a signal can be shifted by multiplying it with another sinusoidal signal:

$$x(t) = A\cos\omega_{in}t$$
$$x(t) = A\cos\omega_{L0}t$$
$$x(t) \times s(t) = \frac{A}{2}cos\,(\omega_{in} - \omega_{L0}) + \frac{A}{2}cos\,(\omega_{in} + \omega_{L0})$$

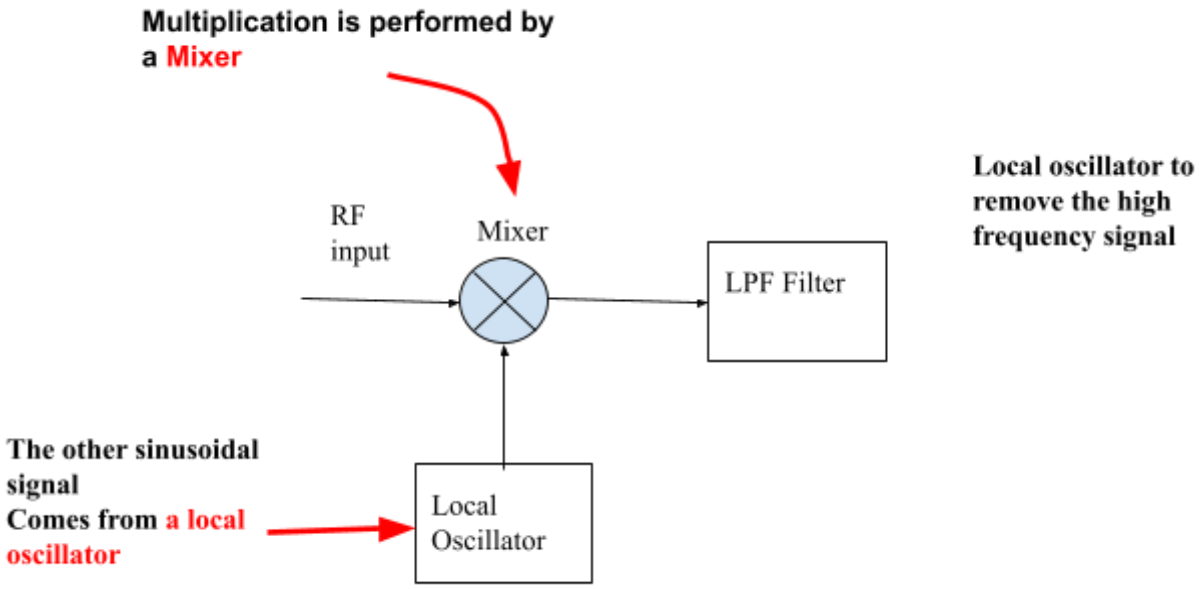


Figure 2.16: The multiplication of a frequency signal with another sinusoidal signal

2.5.2 Homodyne Receiver

Homodyne receiver is a special type of single stage frequency converter.

- Uses same carrier as Tx to down convert signal
- Provide coherent detection (because it uses an LO that synchronize with the transmit)
- Translates spectrum around carrier to DC (ω_{in} and ω_{C} are the same)

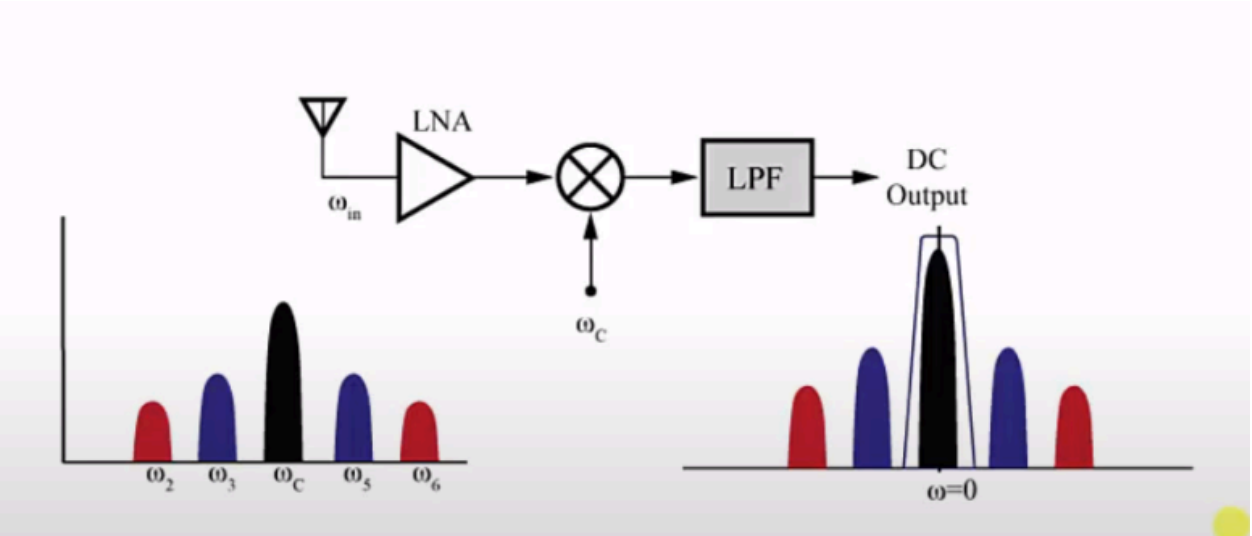


Figure 2:17: Homodyne receiver translation of a spectrum around carrier to DC

2.5.3 Benefits

- Reduced system complexity (Single mixer and filter at low frequency)
- Baseband signal is readily available
- High-selectivity (Because you are filtering at a lower frequency)

2.5.4 Disadvantages

- LO leakage causes self mixing that leads to large DC offset
- Need to generate a precise coherent LO

Most practical today due to software radios:

Baseband is sampled by ADC and mixing , filtering done digitally [14].

2.5.5 Historical note

Developed in 1932 after superheterodyne (1918) to be a better / simpler radio

2.5.6 Heterodyne Receiver

By down-converting the radio-frequency signal (RF) to a lower intermediate frequency (IF), better selectivity can be achieved and SNR is improved

The idea here is that we take our incoming signal and we down convert it with an LO and in this case it is not equal to our input, and what this does is it puts our input signal at a lower frequency that allows us to basically process that signal in an easier format [14].

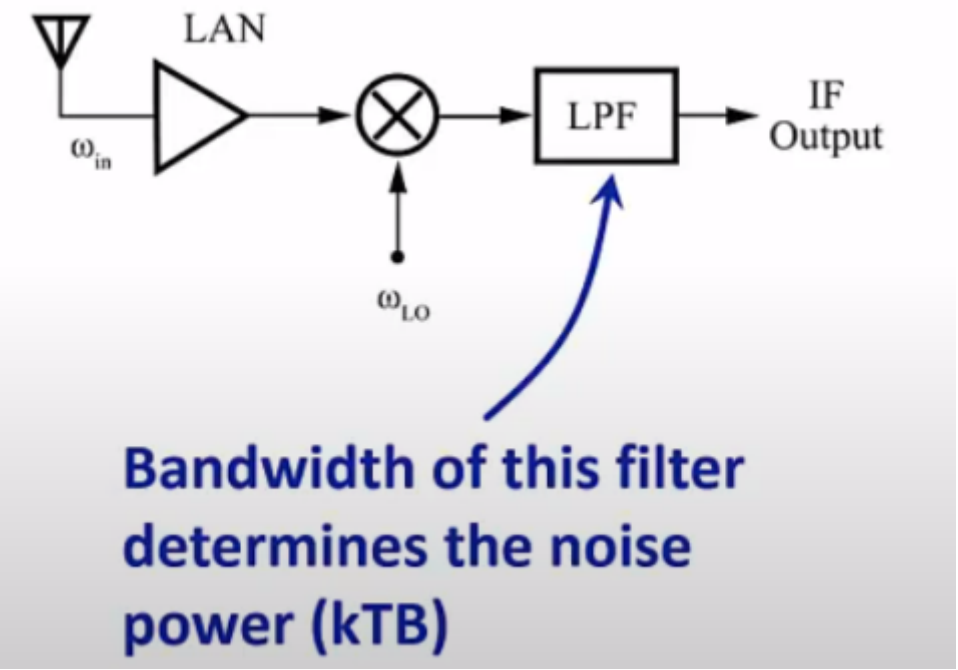


Figure 2.18: Heterodyne receiver down-converting the radio-frequency signal (RF) to a lower intermediate frequency (IF)

2.6 Fractional-Order PLLs

With the advent of fractional calculus in control systems, PLL designs witnessed a paradigm shift. Podlubny's Fractional Differential Equations [3] introduces the mathematical underpinnings of fractional calculus and its application in various control systems, including PLLs. This book is pivotal in understanding the theoretical framework that supports the use of FO-PLLs, which offer improved control over phase noise and stability through non-integer order elements in their feedback loop.

Transitioning to Advancements to Fractional-Order PLLs, recent studies have illuminated the shift from integer-based PLL designs to fractional-order counterparts. This transition, underscored by a surge in computational power and algorithmic sophistication, has been marked by a notable improvement in the control and flexibility of signal processing. Literature from the past decade, Fractional/Integer-N PLL Basics Edited by Curtis Barrett [5] in particular, has delved into the mathematical models and theoretical frameworks that underpin FO-PLLs, showcasing their superiority in various performance metrics over traditional PLLs.

2.7 Performance Metrics in Communication Systems

The literature extensively discusses Phase Noise and Stability, identifying these aspects as crucial performance indicators in PLL design. Comparative studies between integer and fractional-order PLLs reveal a marked improvement in lowering of the division ratio, lowering phase noise, and improving dynamics by increasing the reference frequency. There is the potential to improve switching speed due to faster phase detector frequencies and possibly wider loop bandwidths when fractional-order designs are employed. Such discussions are instrumental in understanding the technical merits and limitations of PLL technologies in real-world applications.

Similarly, literature focusing on Lock Time and Frequency Stability delves into the dynamic performance of PLLs under varying operational conditions. These studies provide empirical evidence and theoretical analysis on the enhancements fractional-order systems offer, particularly in terms of faster lock times and superior frequency stability. Fractional-N can be much faster as it allows the possibility of a wider loop bandwidth for similar spur suppression requirements.[5]

2.8 Debates and Contradictions

There are various debates and contradictions surrounding the adoption of Fractional-N PLLs in comparison to integer-N architectures. Advocates of Fractional-N PLLs highlight their potential to significantly improve phase noise performance while only slightly increasing complexity. This improvement is achieved through a reduction in division ratio, enabled by the use of higher reference frequencies (Fr), which widens the loop bandwidth and enhances switching speed.

Moreover, Fractional-N PLLs offer high resolution in applications where integer-N PLLs falter due to excessively high division ratios. The compensation accuracy of Fractional-N design enables economical single-loop solutions, avoiding the need for complex multi-loop designs.

However, it's essential to recognize that integer and fractional PLL technologies complement each other. While Fractional-N PLLs offer significant advantages, they are not positioned to replace integer-N PLLs entirely. Both techniques offer speed enhancements, but Fractional-N PLLs generally result in faster lock times due to higher reference frequencies. Despite the potential for slightly increased complexity, Fractional-N PLLs maintain comparable power consumption, package size, and cost to integer-N PLLs.

While Fractional-N PLLs may exhibit a more complex phase detector and potentially lose some noise performance, the practical improvement in phase noise is typically half of the theoretical potential. As such, the future direction of PLL technology may see a significant shift towards Fractional-N PLLs, driven by their superior performance metrics and potential for broader market adoption.[5]

2.9 Future Directions and Technological Gaps

Emerging trends in the literature point towards novel applications of FO-PLLs and their potential integration with cutting-edge communication technologies. However, despite these advancements. Identified Gaps remain, especially in long-term reliability studies, economic analyses, and scalability assessments. These gaps not only highlight areas ripe for future research but also underscore the ongoing need for innovation and empirical validation in the field.[5]

2.10 Conclusion

The detailed examination of PLL technology, from its conventional implementations to the innovative realm of fractional-order designs, reveals a trajectory marked by significant advancements and persistent challenges. Through the lens of Homodyne FM receivers, this chapter has synthesized key discussions, debates, and scholarly contributions that define the current state of the art. The identified gaps and emerging trends suggest not only a rich area for future research but also a testament to the dynamic nature of communication technology development. This backdrop sets the stage for further inquiry into the application of FO-PLLs, aiming to contribute to the

broader discourse and address some of the outlined research voids through theoretical and simulation-based analysis.

Chapter 3: Study and Analysis of PLL_VHF with measurements

PSpice

- SPICE – Simulation Program with Integrated Circuits Emphasis
- Developed by University of California at Berkeley in 1970s.
- A simulation program that models the behavior of a circuit containing analog or mixed A/D devices, used to test and refine your design before implementing on hardware (PCB).
- PSPICE is the most prominent commercial version of SPICE, initially developed by MicroSim (1984), but now owned by Cadence Design System. Pspice is now a component of the OrCAD Product Family (including Capture CIS, PCB Editor, Pspice, Layout Plus ...)

3.1 Measurements in the temporal domain

The phase detector of Figure 2.4 followed by the low pass filter and interface circuit of Figure 2.6 with the VCO of Figure 2.10, are combined in cascade, in order to constitute the open loop PLL. A simulation of a temporal domain extending up to 900us in steps of 0.1ns is carried out in figure 3.1. The voltage V(C6) across the capacitor C6 in Figure 2.6, as well as the differential output voltages V_{D1} , V_{D2} and the filter output V(Filter) amplified by the amplifier in Figure 2.6. Are reported from Figure 3.1. The transient regime ending at around 110us, is followed by the permanent regime which shows the demodulated signal of 128KHz, unfortunately the permanent regime gives way to a stray voltage which appears around 620us.

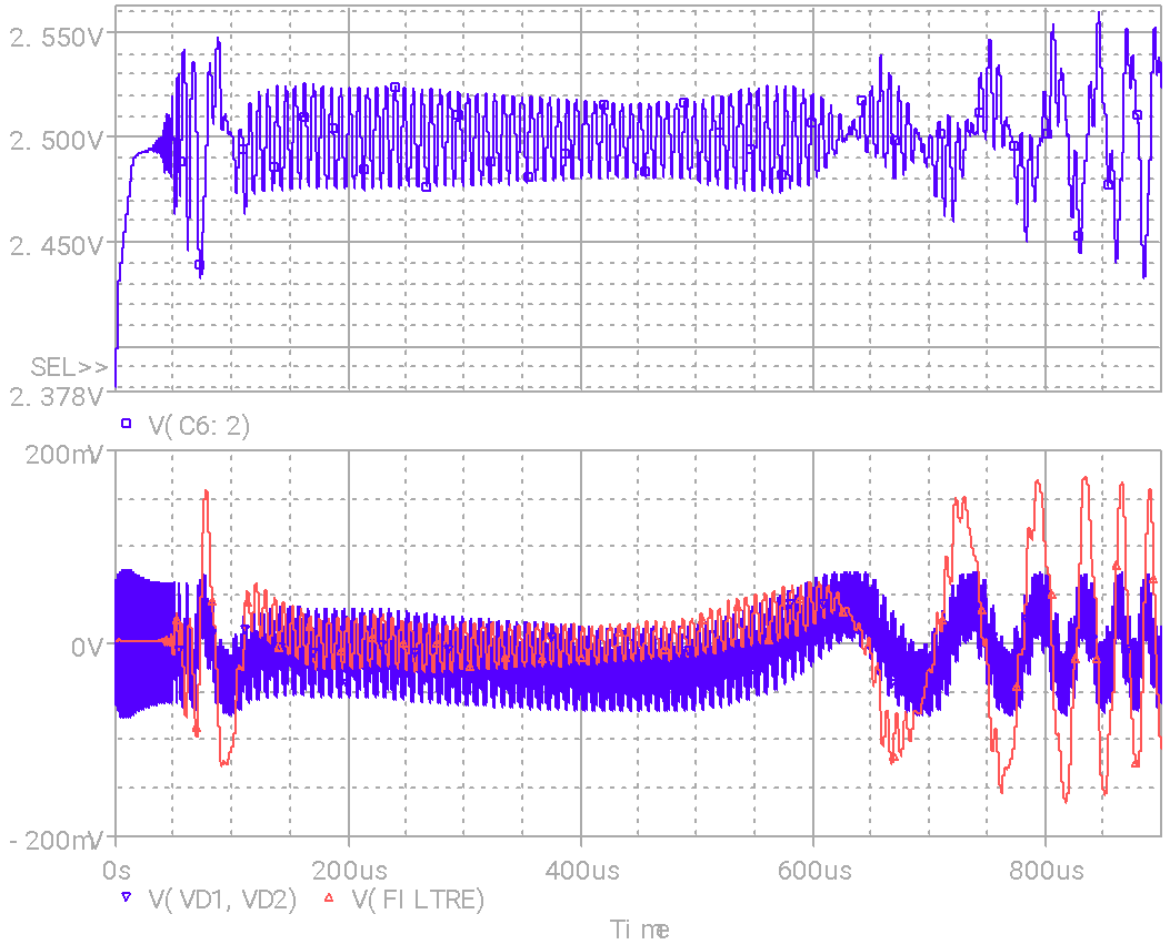


Figure 3.1: Temporal simulation of the PLL in open loop

Or knows that the closed-loop PLL acts as a low-pass filter having the order of its loop filter increased by one, i.e. of order 2. It is hoped that once in a closed loop, the PLL will be able to eliminate the parasites shown in Figure 3.1. The same transient regime of up to 900us of the closed loop PLL is shown in Figure-3.2. The demodulation of the 128KHz LF signal is done in packets, the steady state of which possibly begins from the instant 800us.

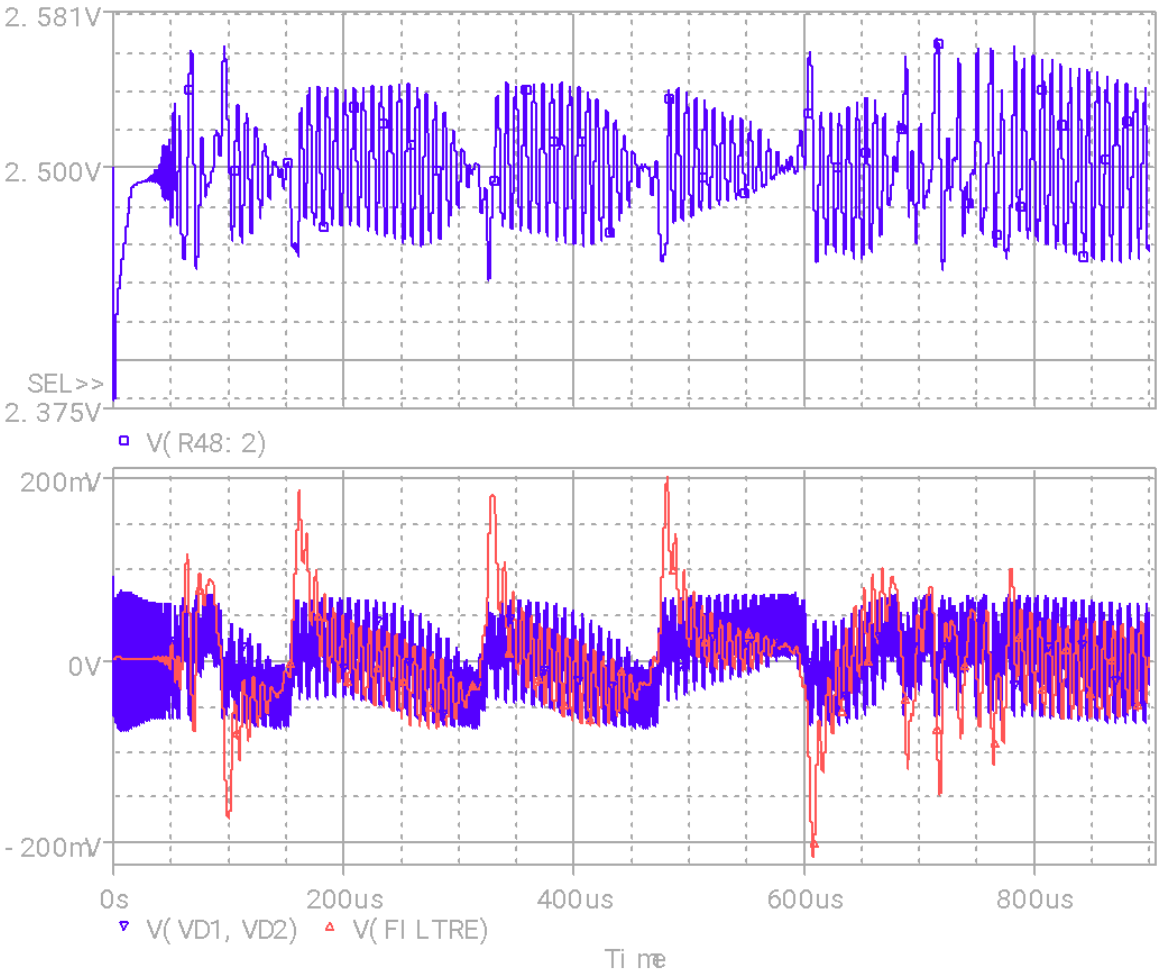


Figure 3.2: Transient regime of the PLL in closed loop

To ensure, the measurement of this permanent regime is shown in Figure 3.3 from 800µs to 1.5ms. Once again, demodulation is carried out discontinuously in packets. The AD834 phase detector is incriminated by this erroneous operation of the PLL, because of its imperfections in particular, the voltage and especially the possibly poorly compensated offset. PSpice offers theoretical components, such as multipliers, in its libraries.

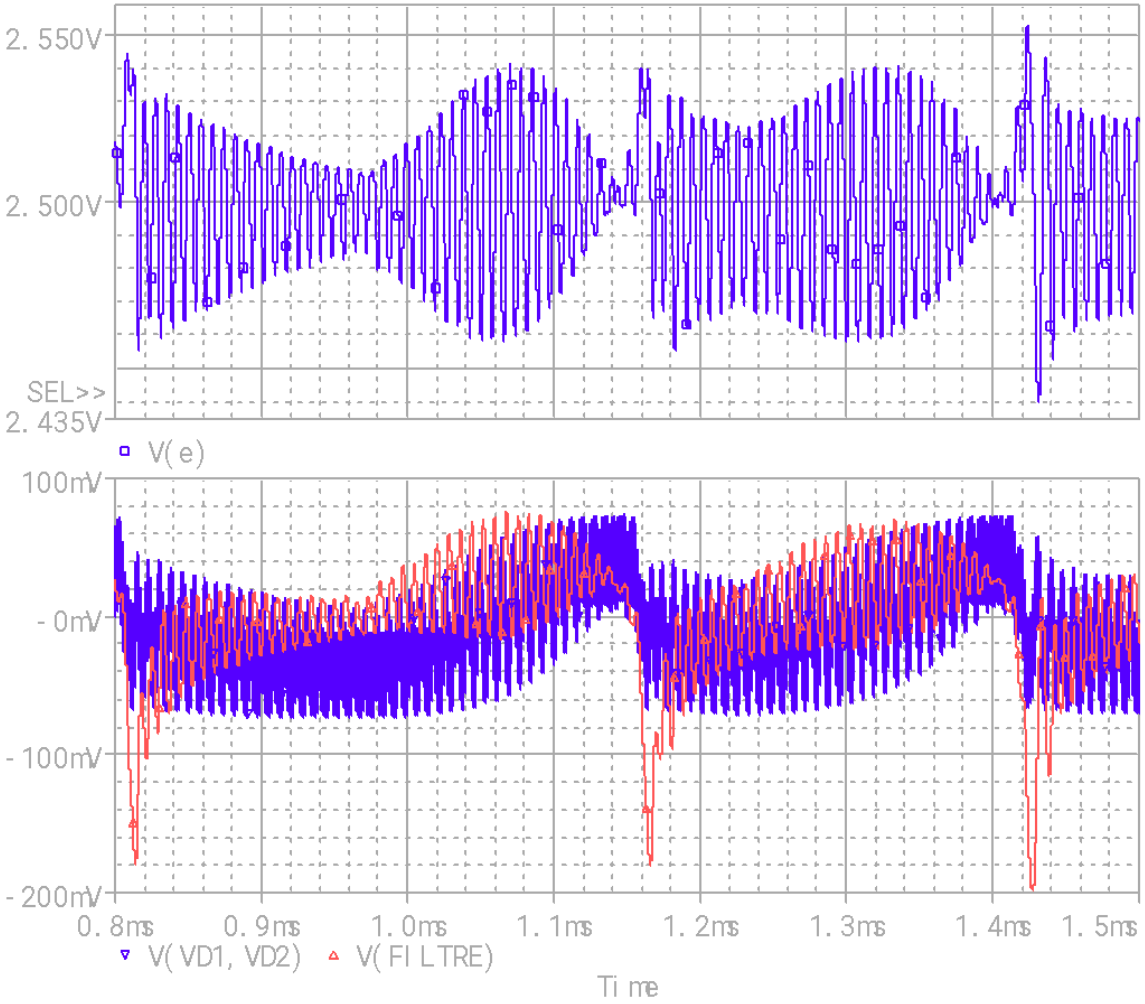


Figure 3.3: Permanent regime of the PLL in closed loop

3.2 Multiplier ABM2I

Among the multipliers offered by PSpice, the ABM2I component was selected which is closest in its operation to that of the AD834 circuit. Consist converts the product of the two input voltages into a proportional output current.

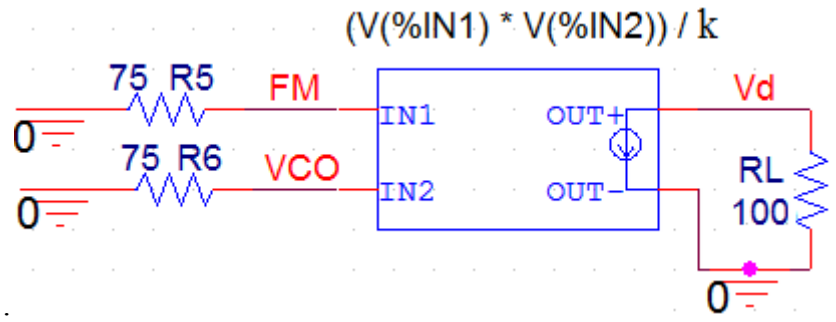


Figure 3.4: ABM2I component as phase detector

It is equipped at its two inputs with resistors 75Ω like the AD834, and at its asymmetrical output with a resistor R_L= 100Ω by analogy still with AD834. The transfer function of such a phase detector can be written:

$$I = \frac{V_{FM} \cdot V_{VCO}}{K} \quad \text{.....(3.1)}$$

With a coefficient K in V. Ω. The value of this coefficient will be fixed later. The availability of an output defined relative to the ground of the new phase detector, greatly simplifies the circuits which follow it. Apart from the VCO circuit in Figure 2.10 which is retained, the simple RC filter is followed by a single op-amp buffer stage mounted as a follower. The primary of the transformer has a ground terminal (instead of -vcc).

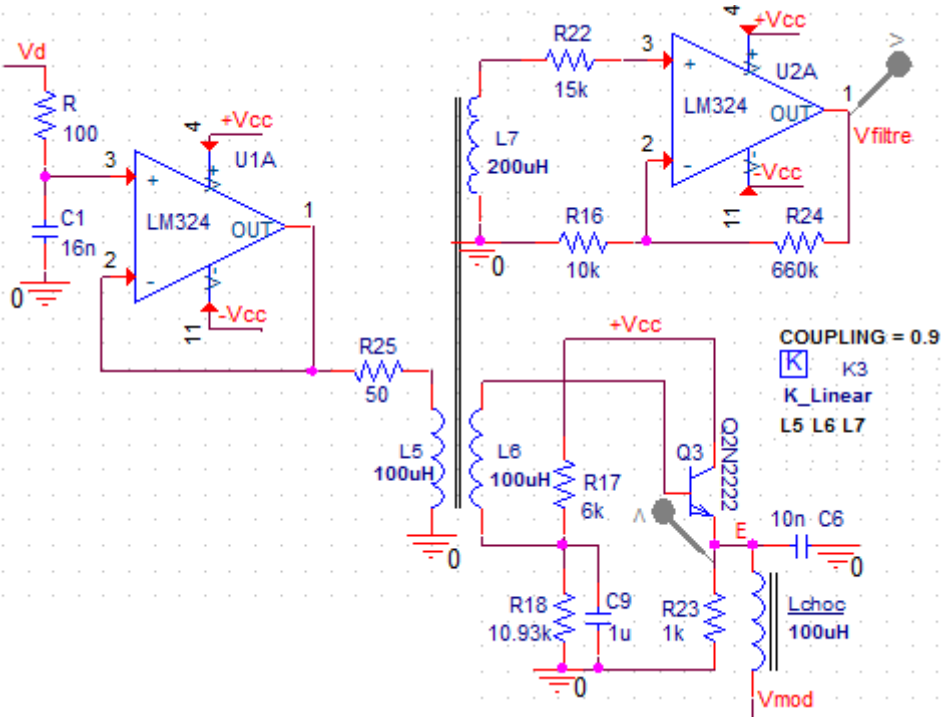


Figure 3.5: Modified filter assembly + VCO interface

Remains connected to two secondaries, one of which powers the op-amp LF amplifier which remains the same as in figure 2.6. The VCO interface stage is transformed into a common collector whose calculation of the polarization resistances must maintain a polarization of 2.5V at the emitter, in order to properly polarize the VCO varicap diodes. Thus for a collector card fixed at $I_C = 2,5mA$ with current gain measured at β = 164 .

$$It\ holds\ a\ basic\ current:\ I_B = \frac{2,5m}{164} = 15uA$$

The transmitter voltage being chosen V_E = 2,5V, the emitter resistance becomes:

$$R_E = \frac{2,5V}{2,5mA} = 1K\Omega$$

$$The\ base\ voltage\ rises\ to\colon\ V_B = 2,5 + 0,7 = 3,2V\,.$$

For better voltage stability V_E= 2,5V polarization of the varicap diodes of the VCO, the stability factor is fixed at $S_I = 5$, from the basic equivalent resistance:

$$R_B = \frac{(S_I - 1)R_E}{1 - \frac{S_I}{\beta}} = \frac{4K}{1 - \frac{5}{164}} = 3,9K\Omega.$$

Thévenin's theorem applied to the basic bridge gives:

$$E_{th} = R_B I_B + V_B = 3.9K \times 15u + 3,2 = 3,3V$$

Which allows us to calculate the ratio between the resistances of the base:

$$\frac{R_{b2}}{R_{b1}+R_{b2}} = \frac{3,3V}{5V} = 0,65 = \frac{R_B}{R_{b1}} \Rightarrow R_{b1} = \frac{3,9K}{0,65} = 6K\Omega$$

$$R_{b2} = \frac{R_{b1}R_B}{R_{b1}-R_B} = 11K\Omega$$

Adjusted to 10,93KΩ in figure 3.5 for V_E = 2,5V.

3.3 New PLL VHF

The detector circuit of figure (3.4) combined with the filter and interface of figure 3.5, as well as the VCO of figure 2.10, allow the closed loop assembly of the PLL.

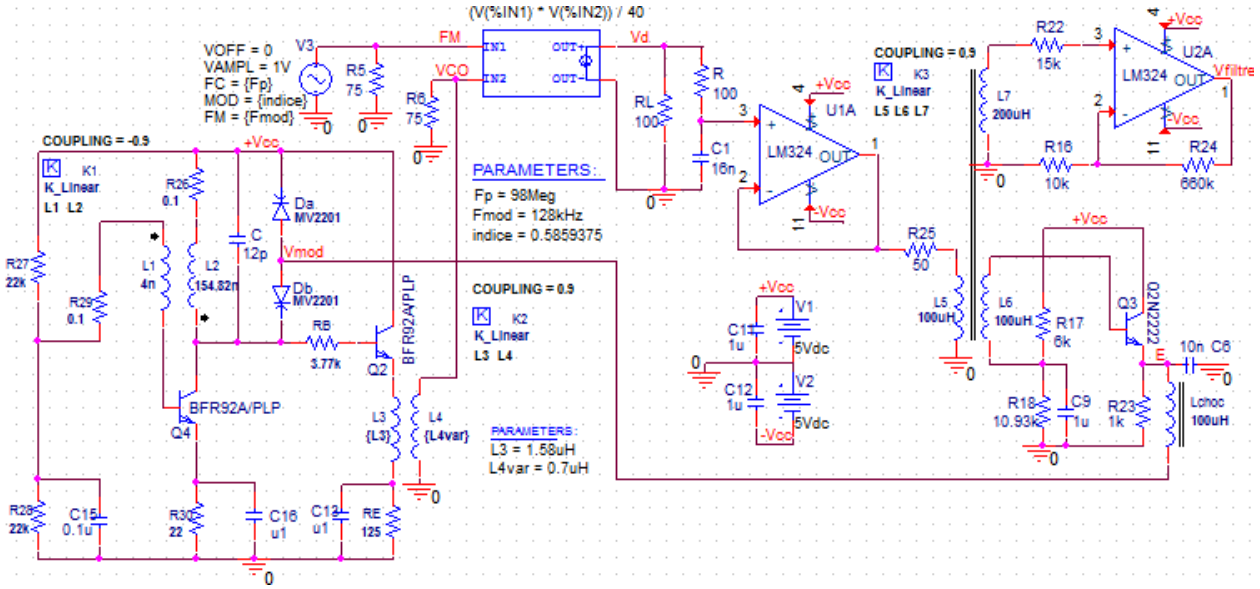


Figure 3.6: Closed Loop PLL

The constant $K = 40V\Omega$ of the multiplier was fixed by trial and error in order to approximate a modulation index $\delta = 0{,}586$ of the modulated VCO signal. same as that fixed to the input FM signal.

3.4 Transfer Function of the PLL

The main functions of the PLL of Figure 3.6 are shown in Figure (3.7) the demodulated output of the FM input signal being taken at the output of the loop filter, the VCO is thus found in the secondary return chain of the PLL loop.The phase detector as well as the loop filter are arranged in cascade in the direct or main chain of the loop.

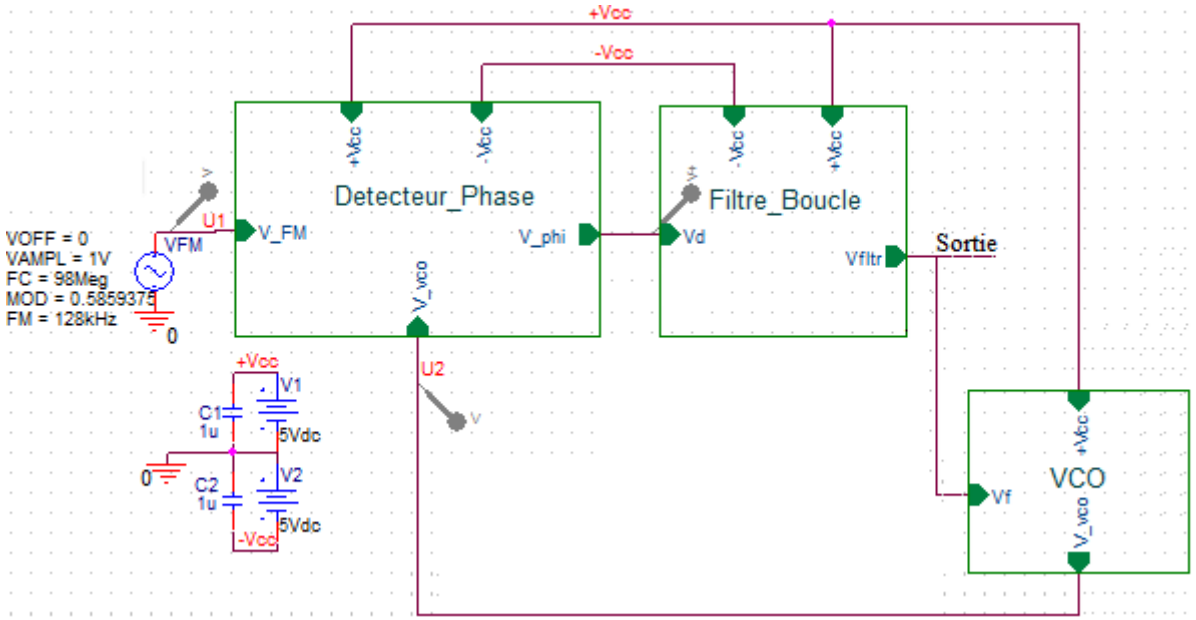


Figure 3.7: Block diagram of the closed PLL in Figure 3.6

The received FM signal is modulated by the information $V_0(t)$ nominal amplitude E_0. Supposedly β , the coefficient of the FM modulator which sets the frequency excursion:

$$\Delta F = \beta E_0 = 75KHz \quad \text{.....(3.2)}$$

The instantaneous frequency of FM varies around the carrier frequency f_p, such as :

$$f(t) = f_p + \beta V_0(t) \quad \text{.....(3.3)}$$

So:

$$w_{FM} = w_P + 2\Pi\,\beta V_0(t) \rightarrow \vartheta_{FM} = \int w_{FM} dt = w_P t + 2\Pi\,\beta \int V_0(t) dt \quad \text{.....(3.4)}$$

Similarly, the second input signal of the phase detector is the VCO signal, the frequency of which varies around its rest frequency w_0 proportional to the filter voltage V_f :

$$w_{VCO} = w_0 + k_0 V_f \rightarrow \vartheta_{VCO} = \int w_{VCO} dt = w_0 t + k_0 \int V_f dt \quad \text{.....(3.5)}$$

When the PLL is locked, the frequencies $\omega_{FM}$and ω_{VCO} become equal while waiting for the minimization of the phase difference between $\vartheta_{FM}$and ϑ_{VCO}, from where :

$$w_0 = w_p = 2\pi \times 98MHz$$
$$w_{VCO} = w_{FM} \Rightarrow \quad 2\pi\beta = k_0 = 11.9 \times 10^6 \, rd/vs$$
$$\beta = 1.89 \times 10^6 (vs)^{-1}$$

With demodulation at the filter output:

$$V_f(t) = V_0(t)$$

Of (3.2), we deduce : E_0 = 39,6mV .

Note well: For sinusoidal information $V_0(t)$ of the expression (2.7), we have φ_{FM} = φ_1 of (2.8).

Likewise ϑ_{VCO}= ϑ_2 of the expression (2.9) with the phase shift $\frac{\Pi}{2}$ coming from the multiplier used as a phase comparator. The Laplace transformation applied to the phase variations of equations (3.4) and (3.5) becomes:

$$\Delta_{\vartheta_{FM}} = 2\pi\beta \frac{V_0(P)}{P} = \frac{K_0}{P} V_0(P)$$

$$\Delta_{\vartheta_{VCO}} = \frac{K_0}{P} V_f(P) \text{.....(3.6)}$$

The transfer functions of each part of the PLL being partially calculated in the previous text, are taken up and completed here:

3.4.1 Phase detector

Assumes a change of variable Δ_ϑ in the expression (2.15) , such as:

$$\Delta_\vartheta = \Delta_{\vartheta_{FM}} - \Delta_{\vartheta_{VCO}} = \frac{\pi}{2} - \Delta_\theta \text{.....(3.7)}$$

Expression (2.15) becomes linear for small phase differences Δ_ϑ, near the PLL hook-up:

$$V_d = V_{phi} = k_d \sin\Delta_\vartheta \simeq k_d \Delta_\vartheta = k_d \frac{\Delta_w}{P} \text{.....(3.8)}$$

With phase detector sensitivity:

$$k_d\left(\frac{V}{rd}\right) = k_m \frac{|V_{FM}| \times |V_{VCO}|}{2} \quad \text{.....(3.9)}$$

In figure 3.6, the static current at the output of the phase detector is fixed at the same value as at the output of the previous detector AD834, i.e. from expression (3.1):

$$I_0 = \frac{|V_{FM}| \times |V_{VCO}|}{40} = 4mA \Rightarrow |V_{FM}| \times |V_{VCO}| = 0,16\,V^2 \quad \text{.....(3.10)}$$

Which gives a static voltage across the load R_L of the detector:

$$V_{d_0} = R_L I_0 = 100 \times 4m = 400mV = k_d \quad \text{.....(3.11)}$$

This static voltage represents the constant k_d from expression (3.9), from which we derive the value of the coefficient of the multiplier:

$$k_d = \frac{k_m}{2}.\,0,16 = 400mV \Rightarrow k_m = \frac{400mV}{80mV^2} = 5V^{-1}$$

3.4.2 Loop filter

$$V_f = V_{filtre} = \frac{V_d}{1+1,6.10^{-6}P} \quad \text{..... (3.12)}$$

3.4.3 VCO

The sensitivity of the VCO being calculated in expression (2.47), it comes with:
$\omega_0 = 98MHz$; $U_0 = 2,5V$; and more precisely in (3.5):

$$\omega_{VCO} - \omega_0 = k_0(V_f - U_0) \Rightarrow \Delta_{\omega_{VCO}} = 11.9 \times 10^6 \times \Delta_{V_f} \quad \text{.....(3.13)}$$

Which represents a linear variation of $\Delta_{w_{VCO}}$ consequent by Δ_{V_f} around the VCO resting point (98MHz ; 2.5V).

The functional block of the Pll is given in figure 3.8. It derives from equations: already established: (3.4), (3.6), (3.7), (3.8), (3.12), and (3.13).

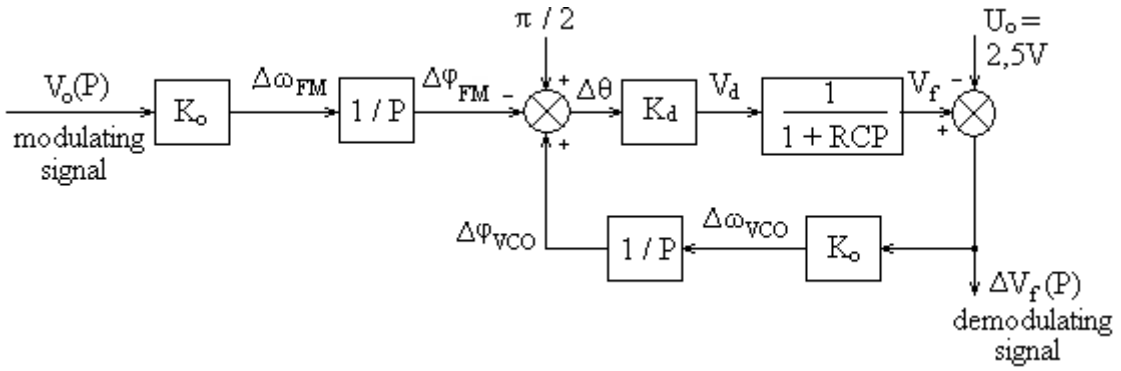


Figure 3.8: Functional block diagram of the pll of Figure 3.6

By neglecting the constants $\frac{\pi}{2}$ and U_0 In figure 3.8, this one simplifies.

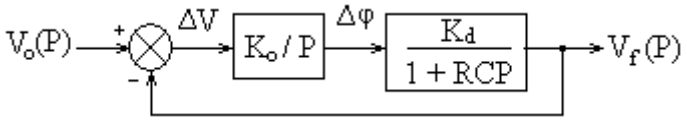


Figure 3.9: PLL unity feedback block diagram

The transfer function of the PLL in open loop becomes:

$$H_{B0}(P) = \frac{V_f(P)}{\Delta V(P)} = \frac{K_0 K_d}{P(1+RCP)} = \frac{\frac{K_0 K_d}{RC}}{P(P+\frac{1}{RC})} = \frac{2975\times10^9(\frac{rd}{s})^2}{P(P+625K)} \quad \text{....(3.14)}$$

The transfer function of the PLL in closed loop is:

$$H_{BF}(P) = \frac{V_f(P)}{V_0(P)} = \frac{\frac{K_0 K_d}{P(1+RCP)}}{1+\frac{K_0 K_d}{P(1+RCP)}} = \frac{\frac{K_0 K_d}{RC}}{P^2+\frac{P}{RC}+\frac{K_0 K_d}{RC}}$$

$$= \frac{2975\times10^9(\frac{rd}{s})^2}{P^2+625K\times P+2975\times10^9} \quad \text{.....(3.15)}$$

The denominator of $H_{BO}(P)$ is the Characteristic equation, which characterizes the stability of the PLL. Outside of zero frequency, the PLL is stable for any working frequency ω. The Bode plots using Matlab of the function $H_{BF}(P)$ are in Figure 3.10. Bode plots show unconditional stability of the PLL.

The cutoff frequency of the closed-loop PLL is measured between two points plotted on each Bode diagram,

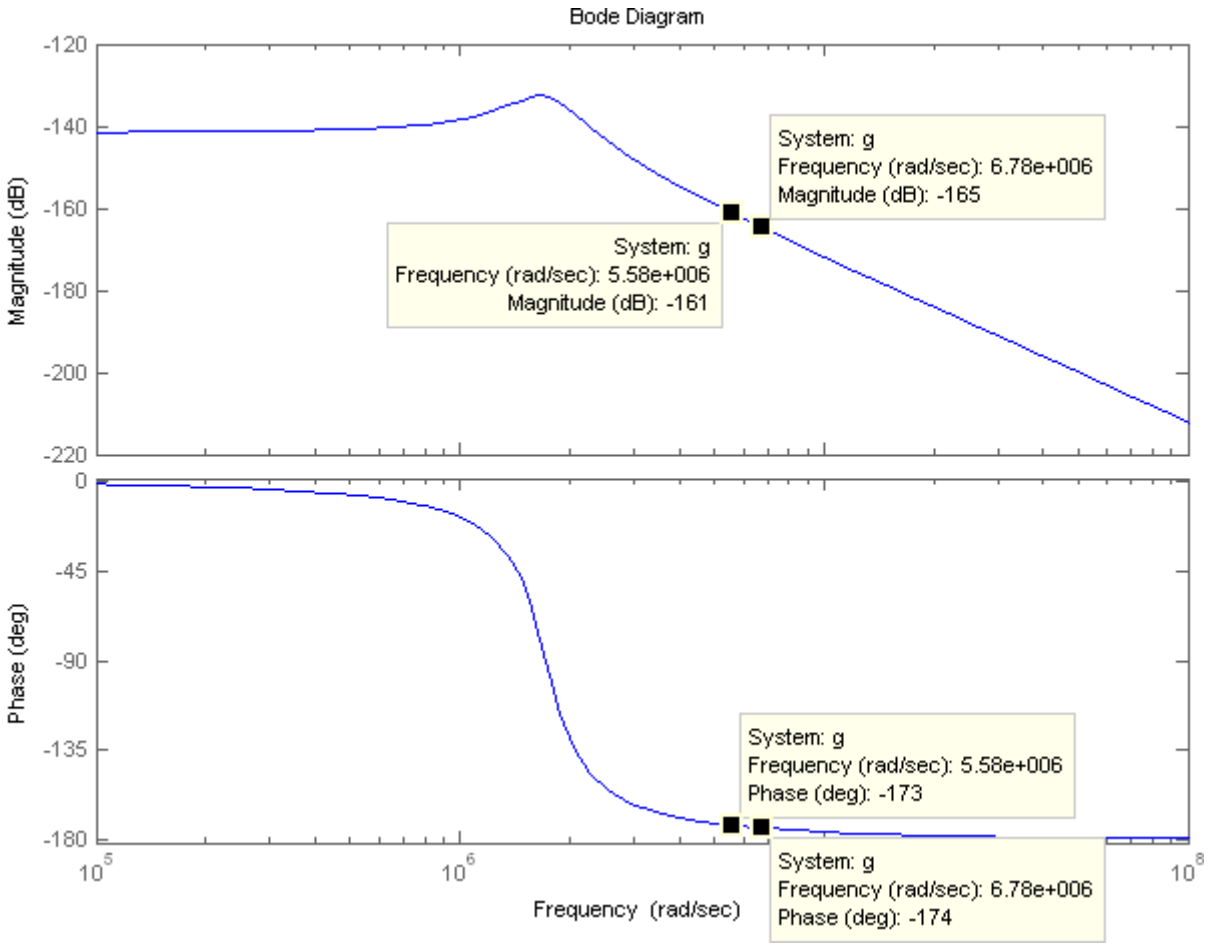


Figure 3.10: Bode plots of the PLL closed-loop transfer function

It corresponds approximately to it, the value $2.6 \times 10^6 \frac{rd}{s}$. or 414KHz and a phase shift of -157^o. The demodulated closed loop test signal is well within the bandwidth of the PLL.

3.5 FM demodulation by PLL

The PLL of Figure 3.6, schematized in Figure 3.7, is subjected to an input FM wave of amplitude 1V, frequency 981HZ, and modulation index $\delta = 0,586$. The transient signal regime of the PLL is presented in figure 3.11, the simulation time is 200us in steps of 0.1ns.

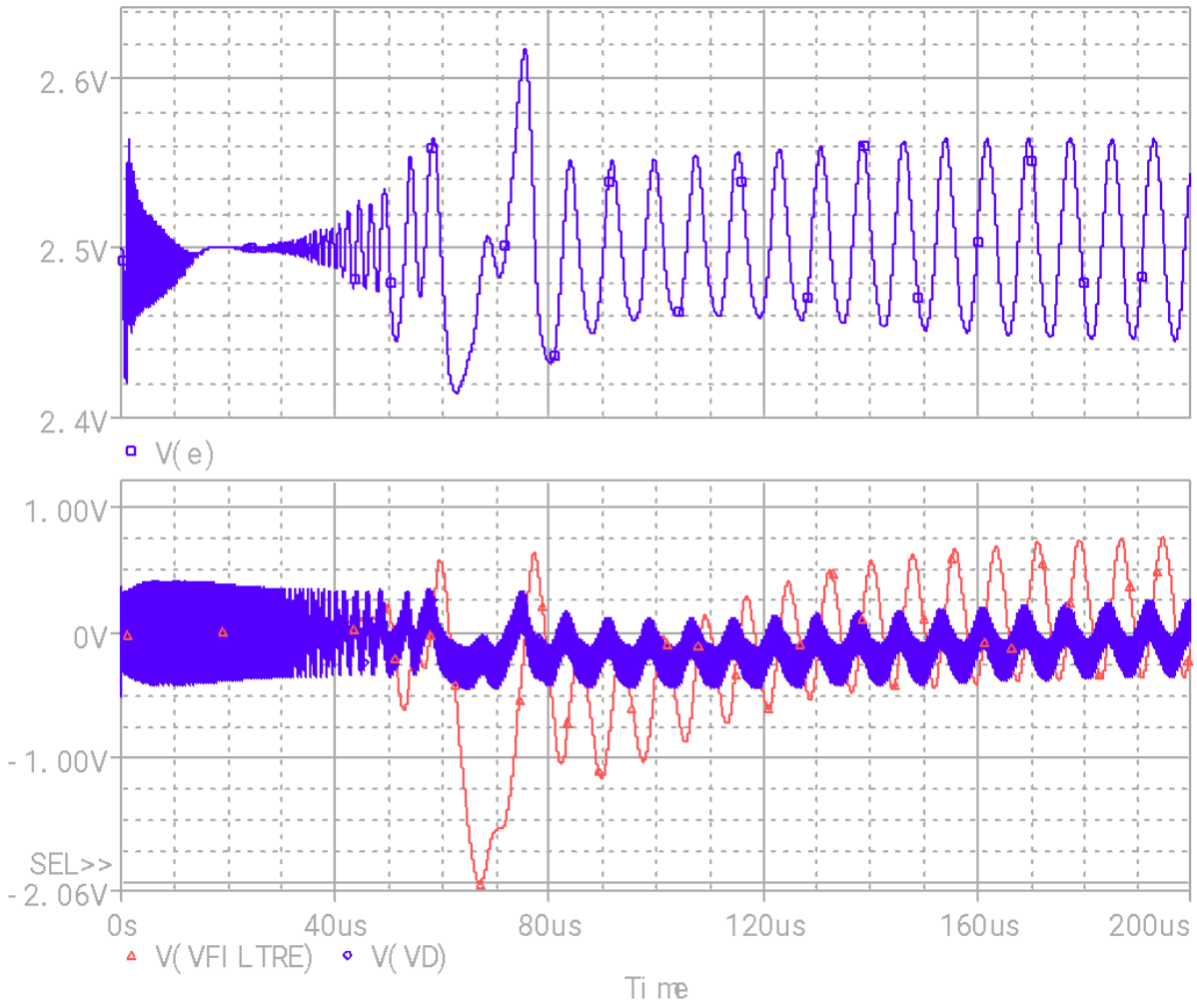


Figure 3.11: Transient regime of the new closed-loop PLL

The filtered and amplified use signal V(Filter) is superimposed on the output signal of the phase detector. While the second filtered signal, which is used to drive the VCO, is measured at the emitter of the VE interface transistor, the restart time of the PLL is estimated at 80us.

The established regime of the same signals of Figure 3.11 is shown in Figure 3.12.

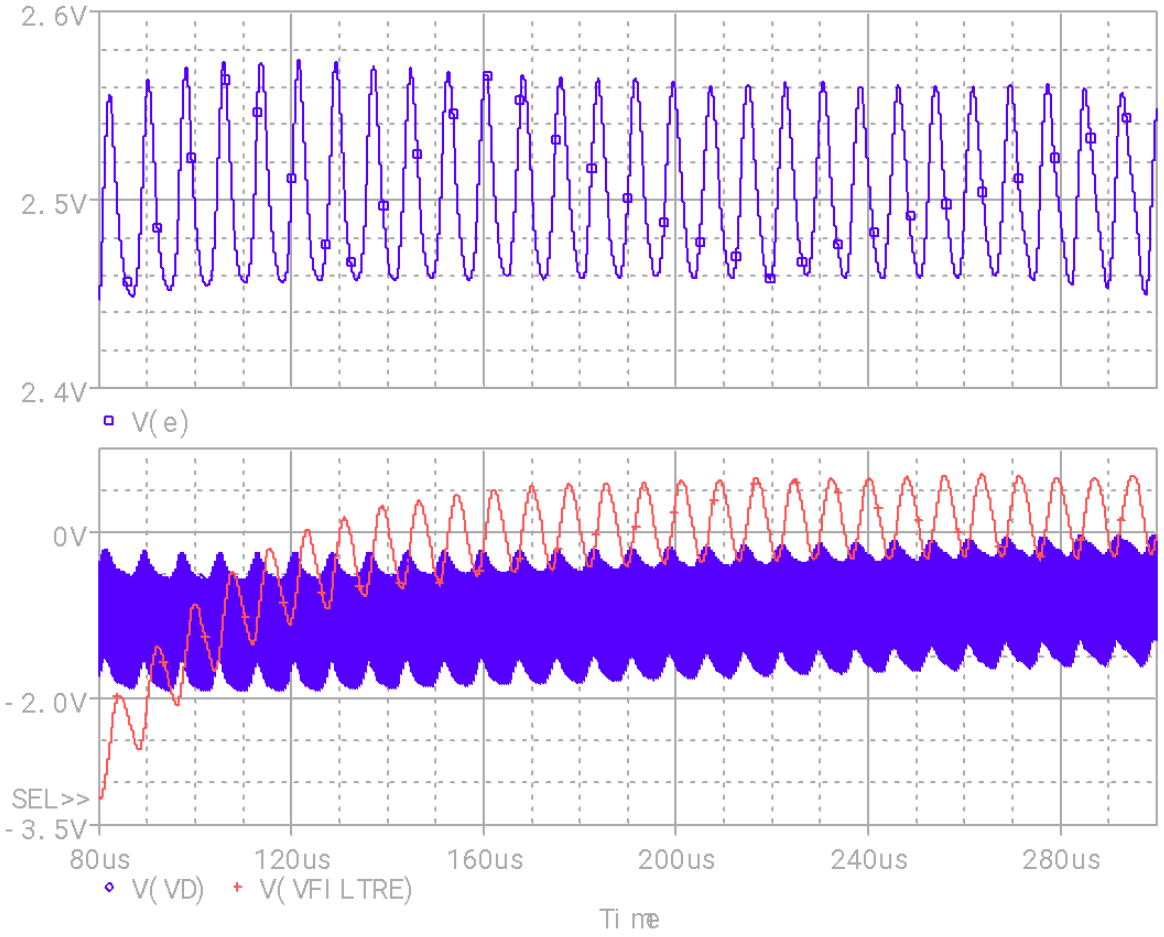


Figure 3.12: Established regime of the new closed loop PLL

The response time based on the V(Filter) output extends to double the estimated time, i.e. 160us. Frequency domain analysis of input signals. V_{FM} and V_{VCO} at the phase detector, shows the three spectral lines expected for narrow-band modulation. The main line at 98 MHZ of the carrier frequency and that of the rest of the VCO, is surrounded by two lateral lines at 98MHZ ± 128KHz.

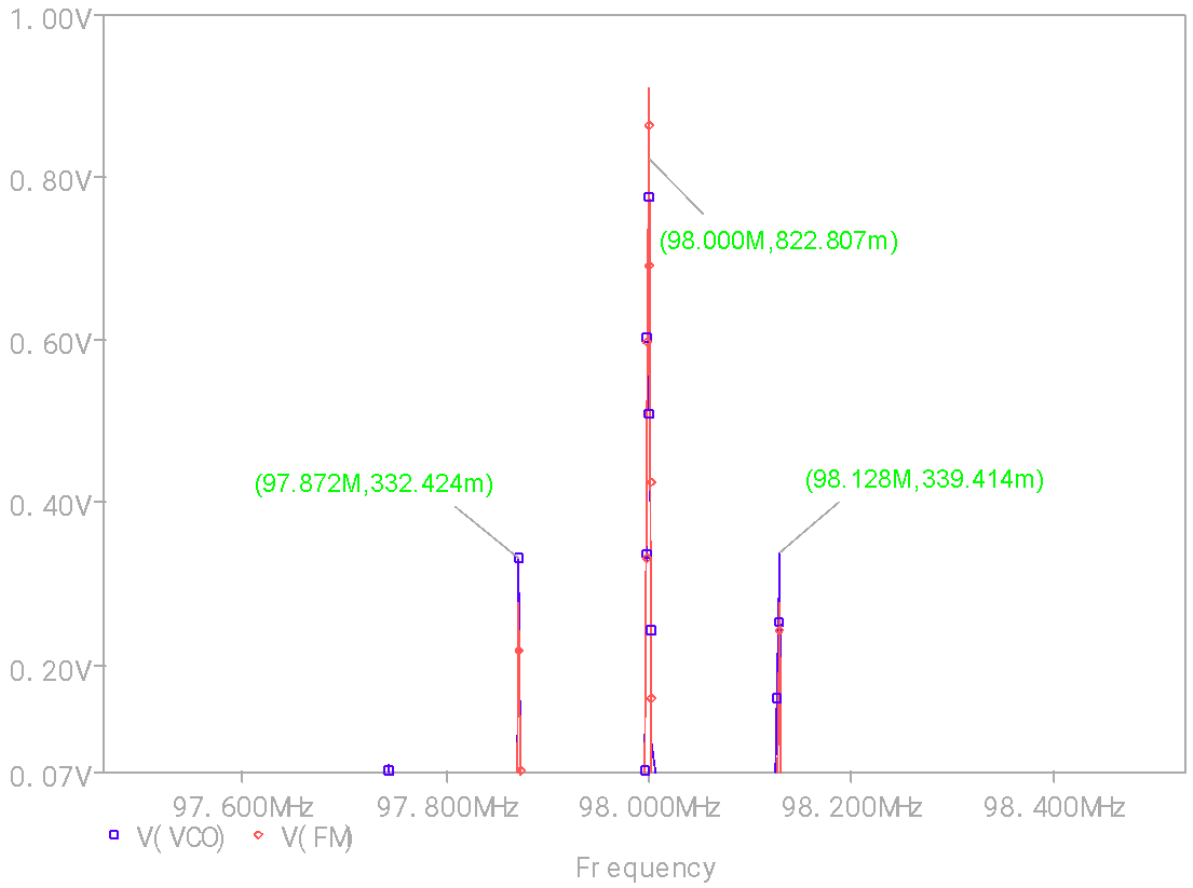


Figure 3.13: FM input and VCO input spectrums at the phase detector

3.6 Property of the PLL produced

The properties or characteristics of the PLL Designed in Figure 3.6 are deduced from its closed loop transfer function $H_{BF}(P)$ Established in equation (3.15).

The expression $H_{BF}(P)$ can be written in the normalized form:

$$H_{BF}(P) = \frac{\frac{K_0 K_d}{RC}}{P^2+\frac{P}{RC}+\frac{K_0 K_d}{RC}} = \frac{\omega_n^2}{P^2 + 2\varepsilon\omega n \times P + \omega_n^2} \quad \text{.....(3.16)}$$

With:

- natural frequency of the PLL: $\omega_n = \sqrt{\frac{K_0 K_d}{RC}} = 1725 \times 10^3 \frac{rd}{s}$
- damping factor: $\varepsilon = \frac{1}{2\sqrt{RCK_0 K_d}} = 0.18$

We recall that the natural frequency is the frequency for which the peak of the amplitude diagram in Figure 3.10 Corresponds. In established regime we have:

$$P \to 0, \textit{ we have } H_{BF}(0) = 1 \Rightarrow V_f(0) = V_0(0). \textit{ which means}$$
$$V_f(t) = V_0(t)$$

The demodulated signal and itself the modulating information signal to be detected.

3.7 PLL optimization

We show that for a second order system, the best compromise is between a possible flat frequency response curve and a system response. The fastest possible, is obtained for a factor:

$$\varepsilon = \frac{1}{\sqrt{2}} = 0.707.$$

The response time of the PLL then became:

$$tr_{min} = \frac{3}{\omega_n}.$$

The own pulsation of the PLL must be chosen equal to the upper limit of the transmitted baseband, Or for a Hi-Fi audio signal sampled for end of digitization:

$$\omega_n = 2\pi fe_{max} = 2\pi \times 48KHz \simeq 302 \times 10^3 \frac{rd}{s} \; With: \; tr_{min} = 10us$$

$(that\ measured\ in\ figure\ 3.11\ is\ 80us)$

Thus we have:

- $\omega_n^2 = \frac{K_0 K_d}{RC} = 91 \times 10^9$
- $4\varepsilon = \frac{1}{RCK_0 K_d} = 2$

Supposedly:

$$RC = \frac{1}{\sqrt{2 \times 91 \times 10^9}} = 2.34us \; and \; K_0 K_d = \frac{1}{2RC} = 213 \times 10^3 s^{-1}$$

$$For\ R = 100\Omega\ kept,\ we\ have\ C_b = 23.5nF \simeq 24nF$$

As:

$$K_0 = 11.9 \times 10^6 \frac{rd}{Vs} \rightarrow K_d = \; = 17.9 \frac{mV}{rd} \; of\ equation\ (2.47)$$

From equations (3.9) and (3.10), the constant K of the phase detector (3.1) becomes:

$$K = \frac{17.9m}{\frac{5}{2} \times 4m} = 1.8V\Omega.$$

These optimization settings of the PLL are reported in the circuit of Figure 3.6.

3.7.1 Possible disruption of the PLL

We assume that the frequency ω_{VCO} from the VCO is subject to a disturbance $\delta_{\omega_{VCO}}$ relative to the VCO Rest point:

$$(\omega_0 = 2\pi \times 98MHz\,;\ U_0 = 2.5\,V)$$

Expression (3.13) can be written:

$$\omega_{VCO} = K_0 V_f \ with\ \varphi_{VCO} = \frac{\omega_{VCO}}{P}$$

The frequency disturbance of the VCO is added to the frequency ω_{VCO} in figure (3.8), which modifies the latter according to figure (3.14).

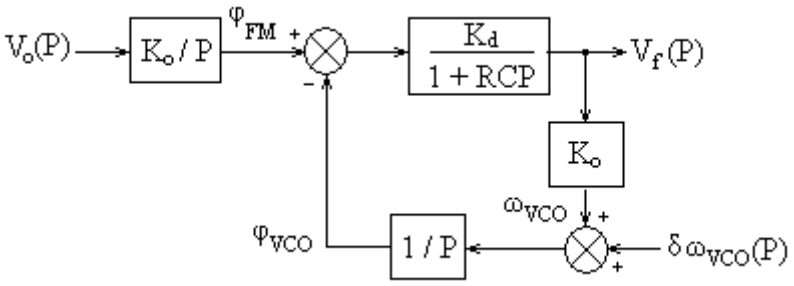


Figure 3.14: Block diagram of the PLL with frequency disturbance

Considering Input Disturbance with Zero Main Input,$V_0(P) = 0$, the PLL operates in regulation mode, the block diagram of which becomes as in figure 3.15.

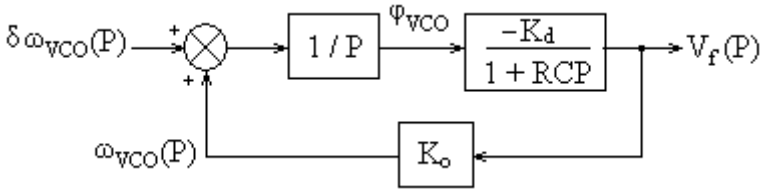


Figure 3.15: Regulation diagram of the disturbed PLL

The minus sign attached to the main chain in Figure 3.15, comes from the fact that:

$$V_0(P) = 0 \rightarrow \varphi_{FM} = 0 \rightarrow \varphi_{FM} - \varphi_{VCO} = -\varphi_{VCO}.$$

The transfer function of the PLL without regulation, figure 3.15, is:

$$\frac{V_f(P)}{\delta\omega_{VCO}(p)} = \frac{-\frac{K_d}{P(1+RCP)}}{1 - K_0 \times \frac{-K_d}{P(1+RCP)}} = \frac{-K_d}{K_0 K_d + P(1+RCP)} \quad \text{.....(3.17)}$$

Thus for an amplitude disruptor frequency step, the variation caused on the output $V_f(P)$ is:

$$V_f(P) = \frac{\Omega}{P} \times \frac{-K_d}{K_0 K_d + P(1+RCP)} \rightarrow V_f(t \rightarrow \infty) = \lim_{P \rightarrow 0} PV_f(P) = -\frac{\Omega}{K_0} \quad \text{.....(3.18)}$$

There is therefore a static error on $V_f(t)$.

3.7.2 Correction of the PLL

In order to eliminate the influence of a frequency disturbance on the PLL, a PI type corrector is said to be introduced into the system which is able to eliminate the static error on $V_f(t)$.

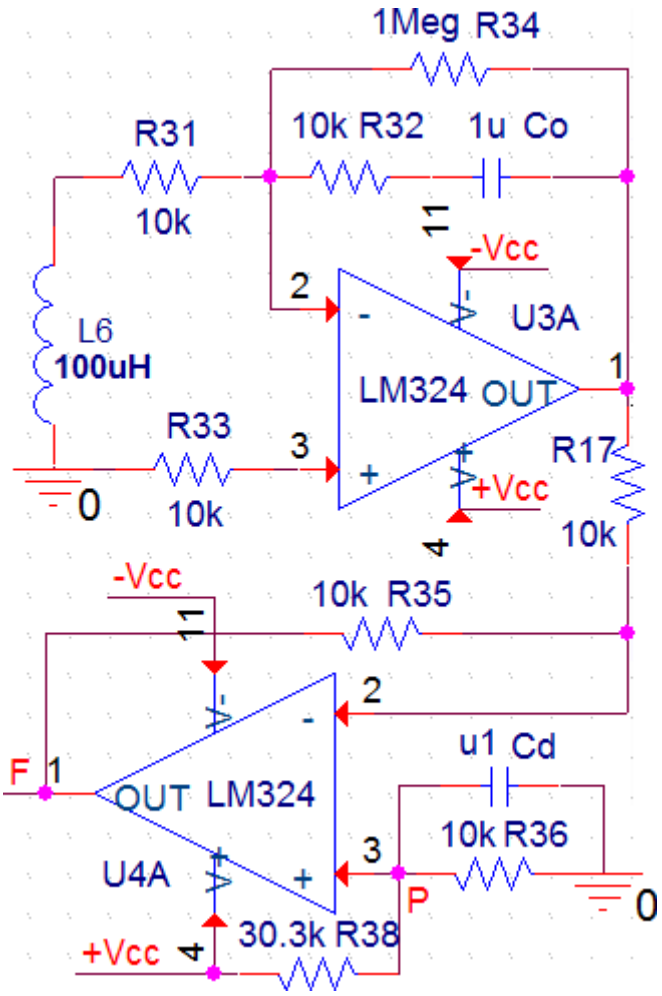


Figure 3.16: PI corrector followed by an inverting amplifier

Resistance R_1 serves to let the bias current coming from the output, and intended for the inverting input of the op-amp. It is chosen large and is therefore neglected in the calculations. The transfer function of the PI corrector is:

$$\frac{S}{e} = -\left(1 + \frac{1}{R_0 C_2 P}\right) = -\frac{1+R_0 C_2 P}{R_0 C_2 P} \quad \text{.....(3.19)}$$

The corrector is to be inserted after the output of the filter, i.e. in the return chain of the PLL. The block diagram of the PLL in figure 3.17 is inspired by that in figure 3.9.

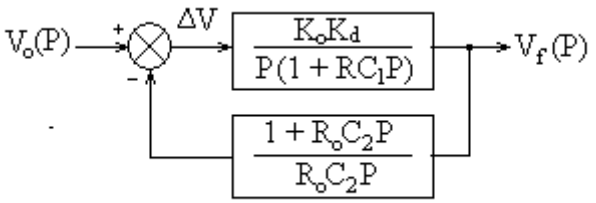


Figure 3.17: Control block diagram of the PLL equipped with the PI corrector

As in expression (3.14), the characteristic equation of the open loop PLL provides information on an unconditional stability of the PLL. The transfer function of the PLL controlled in closed loop becomes:

$$\frac{V_f(P)}{V_0(P)} = \frac{R_0 C_2 P}{\frac{R_0 C_2 p^2}{K_0 K_d}(1+R_0 C_1 P) - (1+R_0 C_2 P)} \quad \text{.....(3.20)}$$

The constant of integration $R_0 C_2$ introduces a low cutoff frequency that does not allow the system to transmit VLF. we then choose: $\frac{1}{R_0 C_2} = 2\pi f_{e_{min}} = 2\pi . 15HZ$ so that the bandwidth of the PLL is at the frequencies:

$$w \gg \frac{1}{R_0 C_2} \; or \; R_0 C_2 P \gg 1 \quad \text{.....(3.21)}$$

With the values found previously:

$K_0 K_d = 213 \times 10^3 s^{-1}$, $R C_1 = 2,34us$, $and\, R C_2 \simeq 10ms$, the Bode diagrams of equation.(3.20) are plotted in figure 3.18.

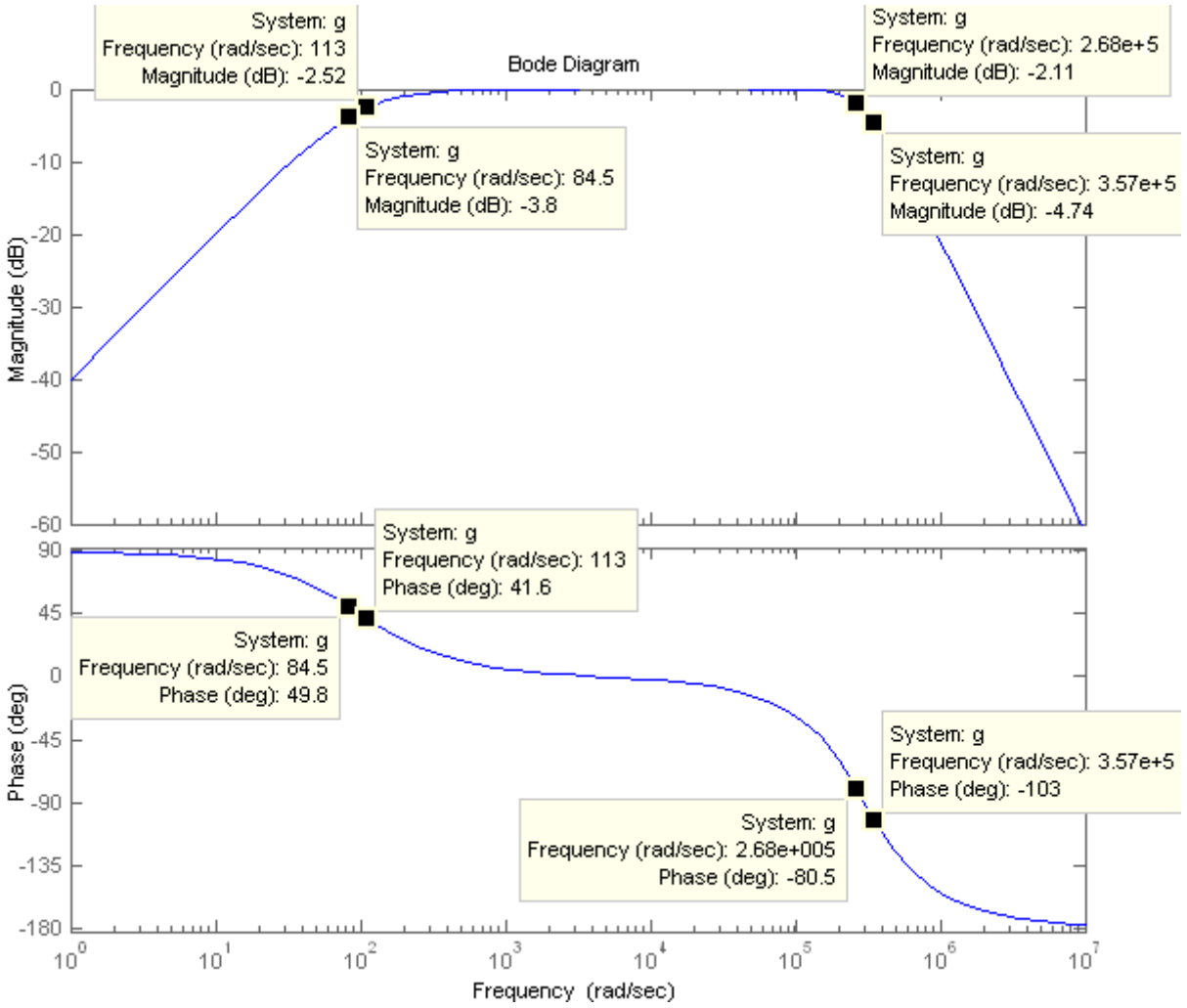


Figure 3.18: Bode diagrams of the corrected PLL

The low cutoff frequency at -3dB is approximately 100rd/s (16Hz) with a phase shift of -135°. The high cutoff frequency at -3dB is approximately $1.5 \times 10^5 rd/s$ (24KHz) with a phase shift brought to -152°. Bode plots show unconditional stability of the PLL.

3.7.3 Regulation of frequency disturbances

Taking into account possible frequency disturbance of the PLL, modifies its block diagram according to figure 3.19, inspired by that of figure 3.14.

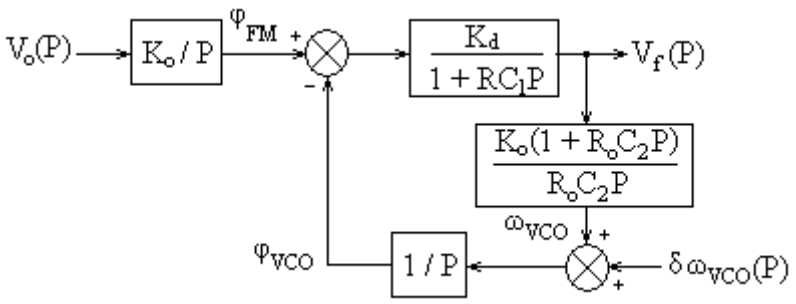


Figure 3.19: Block diagram of Disturbed PLL with correction

For a frequency disturbance input with zero main input, $V_0(P) = 0$, the regulated PLL becomes according to the diagram in Figure 3.20.

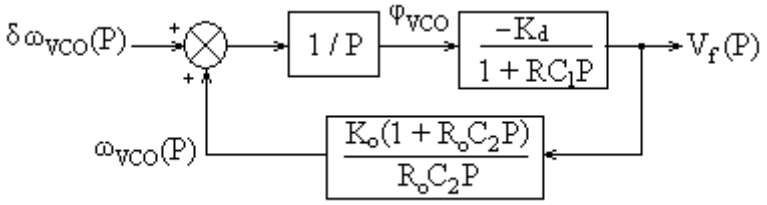


Figure 3.20: Block diagram of regulated PLL equipped with the PI corrector

The transfer function of the system in Figure 3.20 is:

$$\frac{V_f(P)}{\delta\omega_{VCO}(P)} = \frac{+R_0 C_2 P}{K_0(1+R_0 C_2 P) - \frac{R_0 C_2}{K_d} P^2(1+RC_1P)} \quad \text{.....(3.22)}$$

For a disturbance in amplitude frequency step Ω,the variation of the filtered output $V_f(t)$ in steady state will be:

$$V_f(t \to \infty) = \lim_{P \to 0} PV_f(P) = 0 \quad \text{.....(3.23)}$$

Thus, the disturbance no longer has any effect on the output, and we have $V_f(t) = V_0(t)$,even in the event of a disturbance. Figure 3.21 gives a complete view of the PLL-VHF circuit equipped with the PI connector.

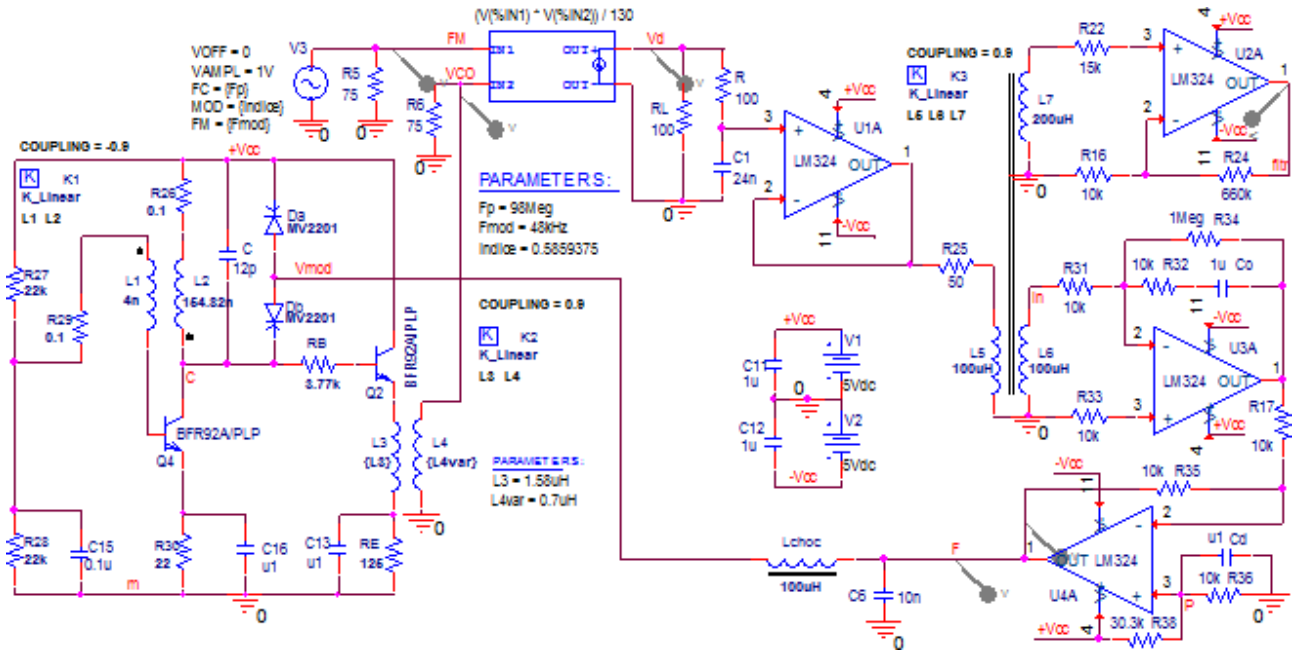


Figure 3.21: PLL-VHF with PI corrector and new VCO interface

The inverting amplifier which follows the corrector, acts as an interface with the VCO in place of the transitory stage, figure 3.5. It must therefore provide the correct polarization of the varicap diodes in addition to the filtered signal at the VCO. For this, a divider bridge placed at the input to the non-inverting input of the op-amp ensures a direct voltage:

$$e_t = \frac{Vcc}{4}$$

The antrum entrance receives a voltage coming from the corrector V_c and from the output of the same op-amp V_s :

$$e_+ = e_- = \frac{Vcc}{4} = \frac{V_S + V_C}{2} \rightarrow V_S = 2.5V - V_c \quad \text{.....(3.24)}$$

The minus sign of (3.24) ensures the phase inversion of $V_C$around the 2.5V polarization. For the same modulation index ensuring a narrow band, the modulating signal is fixed at the upper limit of the base band, i.e. 48KHz with 98MHZ carrier. Thus, low distortion of the demodulated signal is targeted to the detriment of the standard frequency excursion:

$$\Delta F = \delta F = 0.586 \times 48KHz = 28KHz \; instead \; of \; 75KHz.$$

Figure 3.22 visualizes the transient regime obtained, which extends up to 150us.

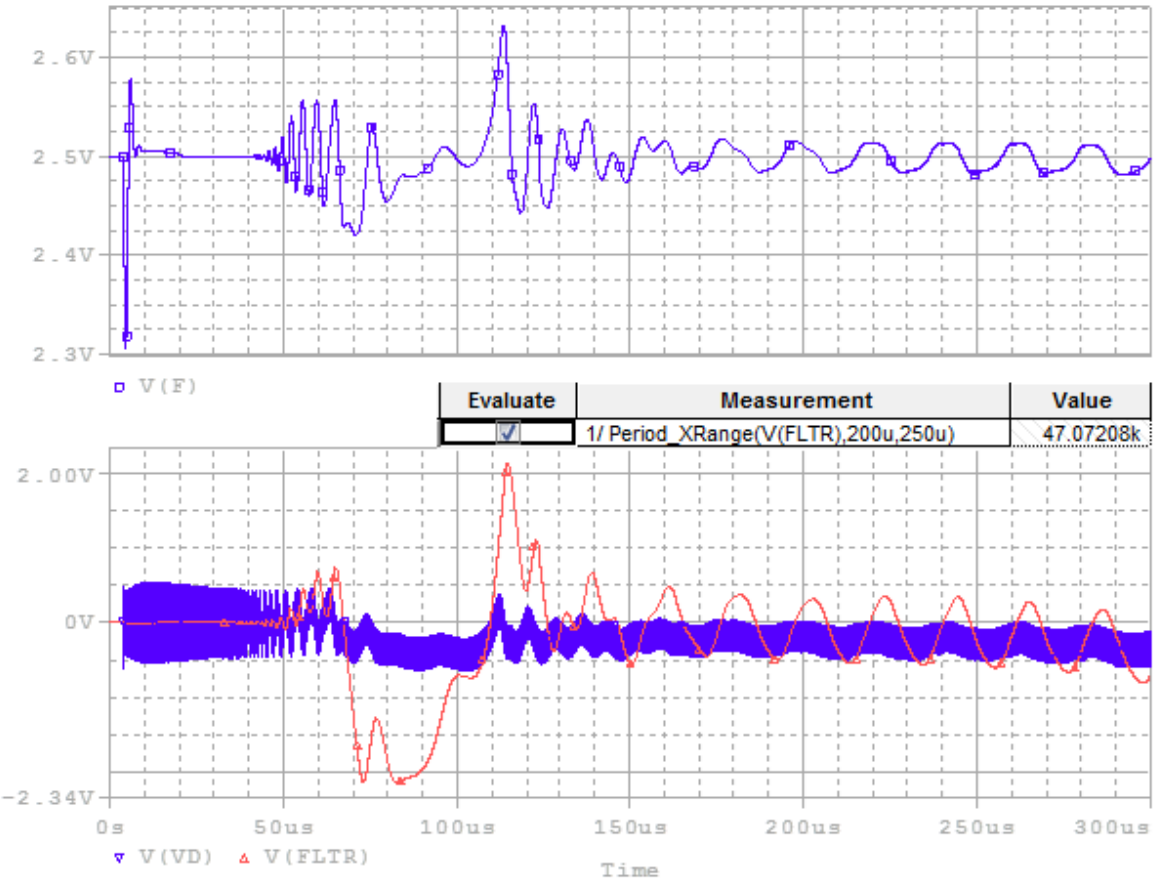


Figure 3.22: Transient regime of the optimized PLL

From there, the established regime began showing the demodulated signal measured at approximately 47KHz lasting a relatively short simulation time. The steady state is taken from Figure 3.23.

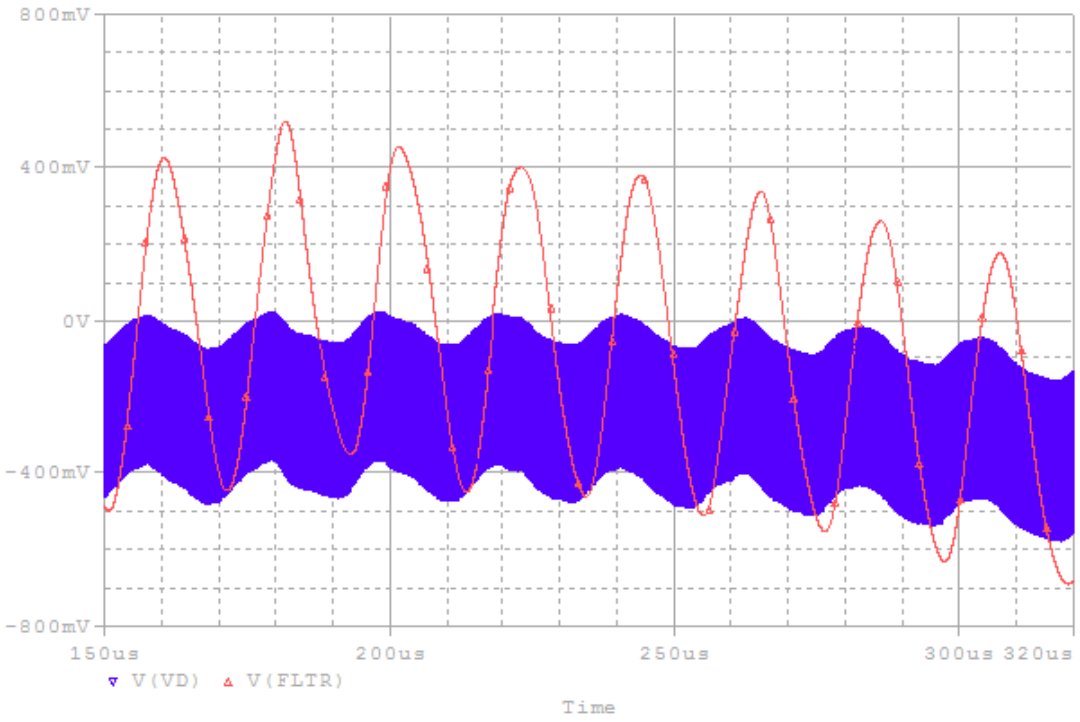


Figure 3.23: Stationary state of the optimized PLL

Whose frequency spectrum is given in Figure 3.24 superimposed on that resulting from the modulated signal received.

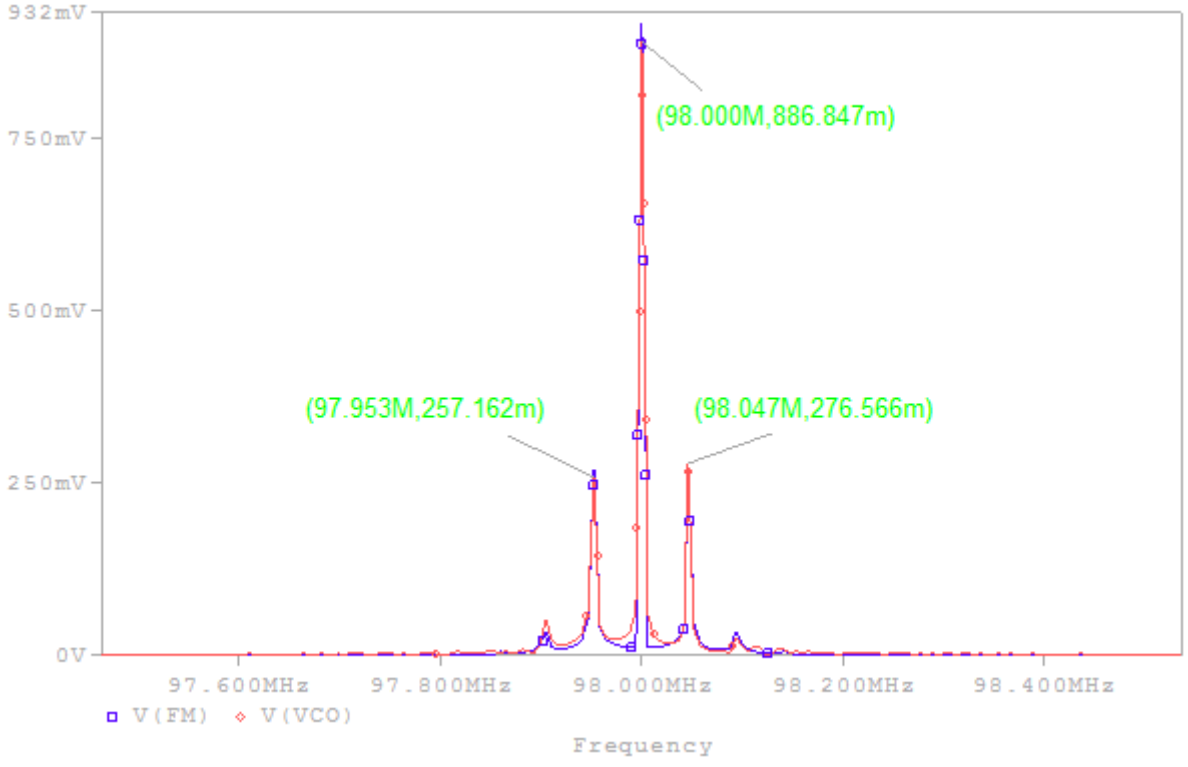


Figure 3.24: Spectrums of FM and VCO signals processed by the optimized PLL

General conclusion

This dissertation has meticulously examined the design, implementation, and performance of Phase-Locked Loop (PLL) circuits within VHF FM communication systems, focusing on key aspects of circuit sizing and temporal behavior analysis. Chapter 1 provided a foundational overview of FM modulation and its significance in communication systems, emphasizing its role in achieving high-fidelity audio transmission and resistance to noise and interference. It also introduced the Phase-Locked Loop (PLL) as a critical technology in frequency synthesis for wireless communication, highlighting its evolution from analog to digital implementations.

In Chapter 2, the research delved into the intricate details of PLL circuit design, ensuring that each component was precisely sized for optimal performance. This thorough approach provided a solid theoretical and practical foundation for the PLL's role in FM communication systems. The chapter underscored the importance of accurate component selection and configuration in achieving desired performance metrics.

Chapter 3 expanded the investigation through temporal domain measurements, presenting a detailed analysis of the PLL's transient and steady-state responses. The simulations highlighted the PLL's ability to demodulate signals effectively. The comparison between open-loop and closed-loop configurations demonstrated the system's potential to suppress stray voltages and maintain signal integrity over extended periods.

While the scope of the research did not extend to fractional-order PLL designs, the findings offer significant insights into the operation of traditional integer-order PLL circuits. The dissertation's comprehensive analysis underscores the importance of precise design and simulation in enhancing the performance of PLL circuits in FM communication systems. The work lays a solid foundation for future research aimed at further improving the stability, efficiency, and resilience of PLL designs in the ever-evolving field of communication technology.

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